

# MS-AAA11 Ver: 1.1

## Intel -Shark bay mobile plamform

### CPU:

Intel - Haswell

### PCH:

Intel - Lynx Point

### GPU:

NVIDIA N14P-GV2

NVIDIA N14M-GE/GL

### OnBoard Chipset:

HD Audio Codec:ALC887

AMP:TPA2008/3009

LAN:RTL8111G

SIO: NCT5533D

eDP to LVDS bridge: PS8625

### Main Memory:

DDR3L (1333/1600MHz) \* 2 (Dual Channel)

### Expansion Slots:

MINIPCI Express (X1) Slot \* 2

### PWM:

Controller:NCP6132 3+2 Phase

Controller:NCP5217 1 Phase

Controller:NCP81172 2 Phase

Controller:NCP1587 1 Phase

Controller:TPS51125 1+1 Phase

### Other:

SATA port: SATA3.0 x1 + SATA2.0 x1

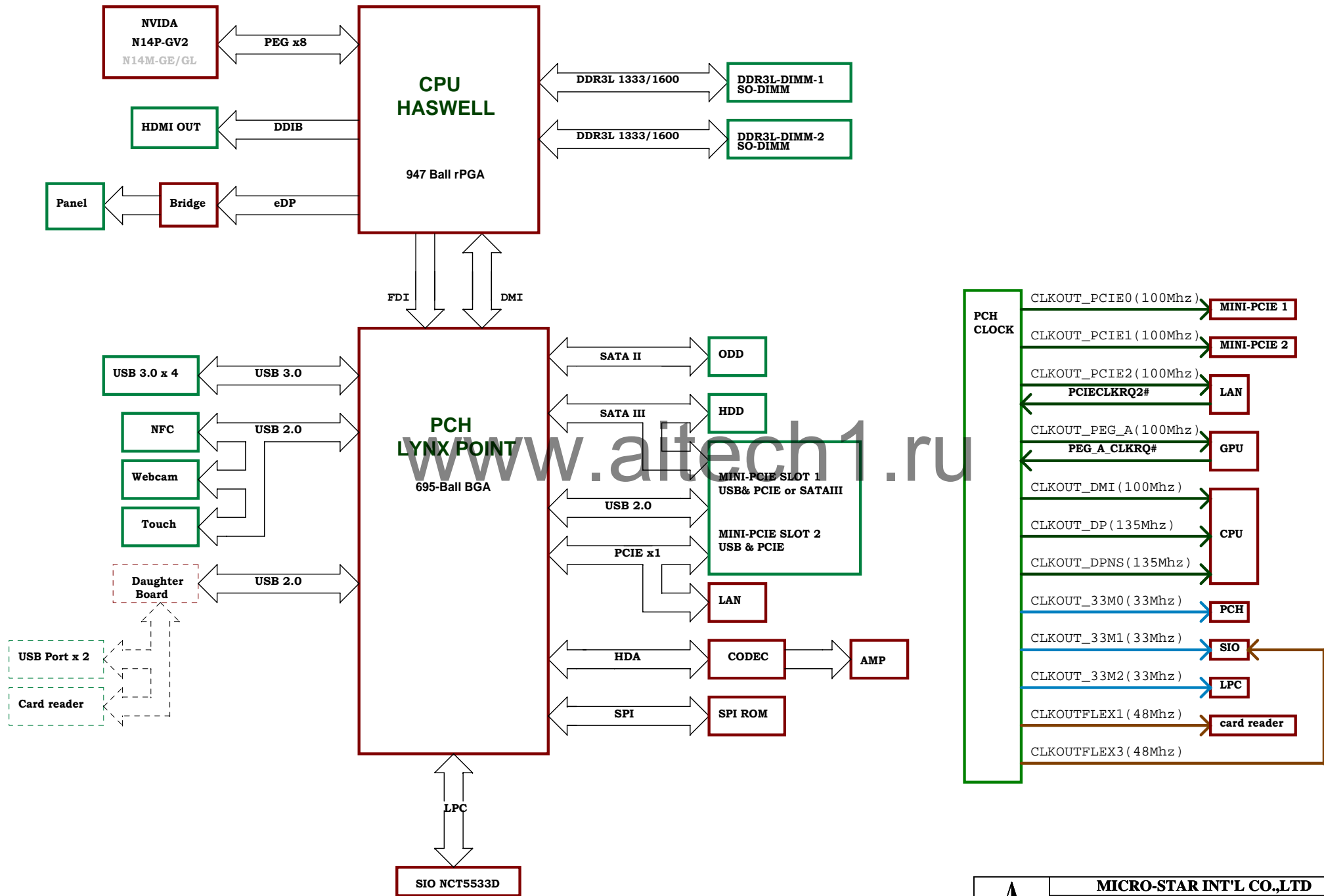
USB port: USB3.0 x4

mSATA: SATA3.0(colay minipcie long card)

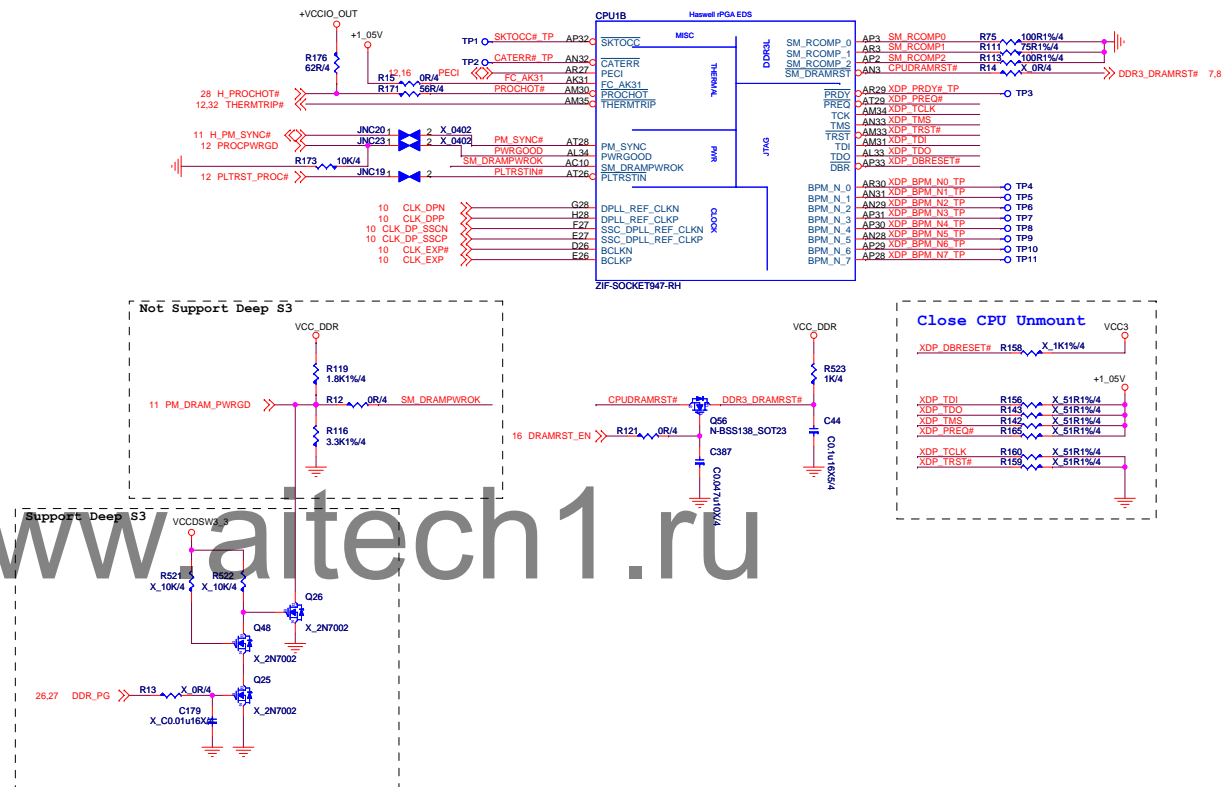
HDMI out x 1

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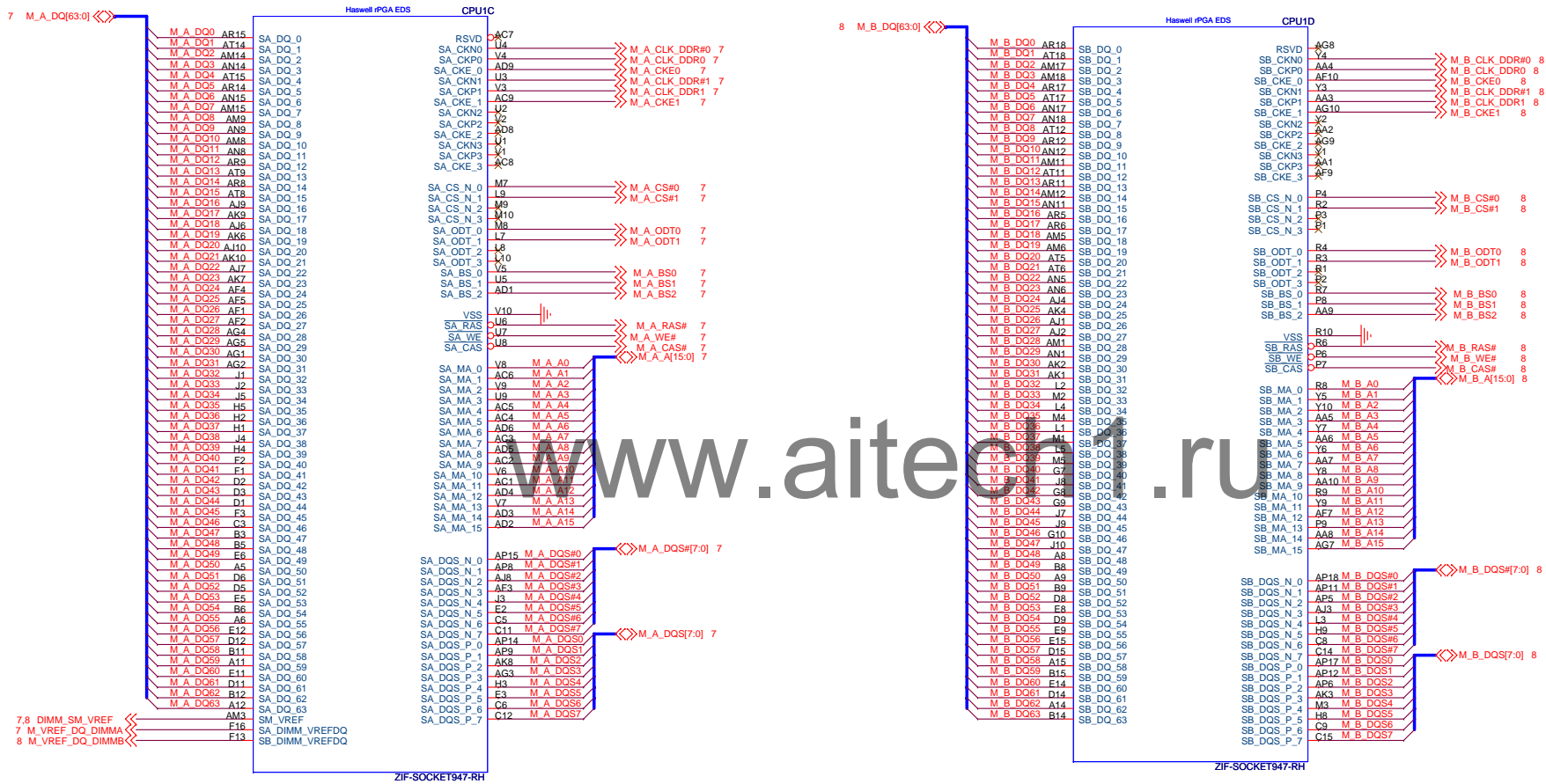
# MS-AAA11



## Haswell Processor (CLK,MISC,JTAG)



## Haswell Processor (DDR3L)



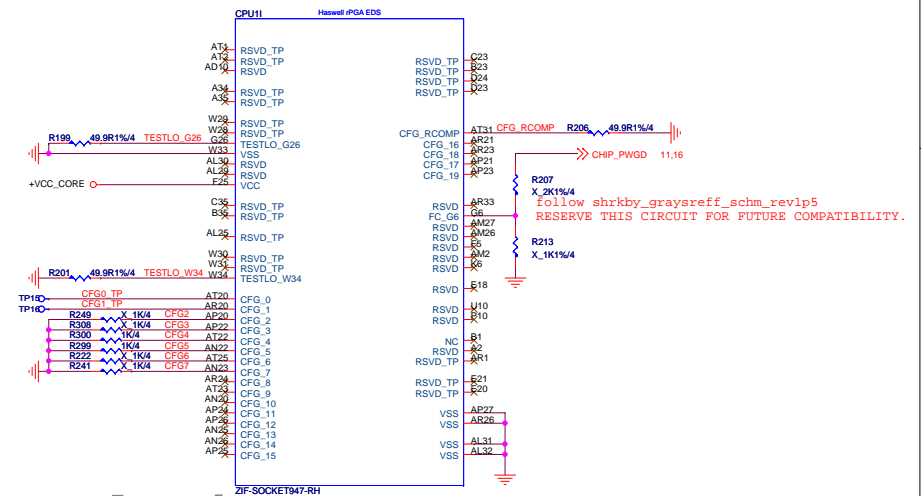
**MICRO-STAR INT'L CO.,LTD**

MS-AAA11

Size	Document Description
Custom	<b>CPU (DDR3L)</b>

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**Haswell Processor (Reserved)**

PCI Express® Static x16 Lane Numbering Reversal

MSR Privacy Bit Feature

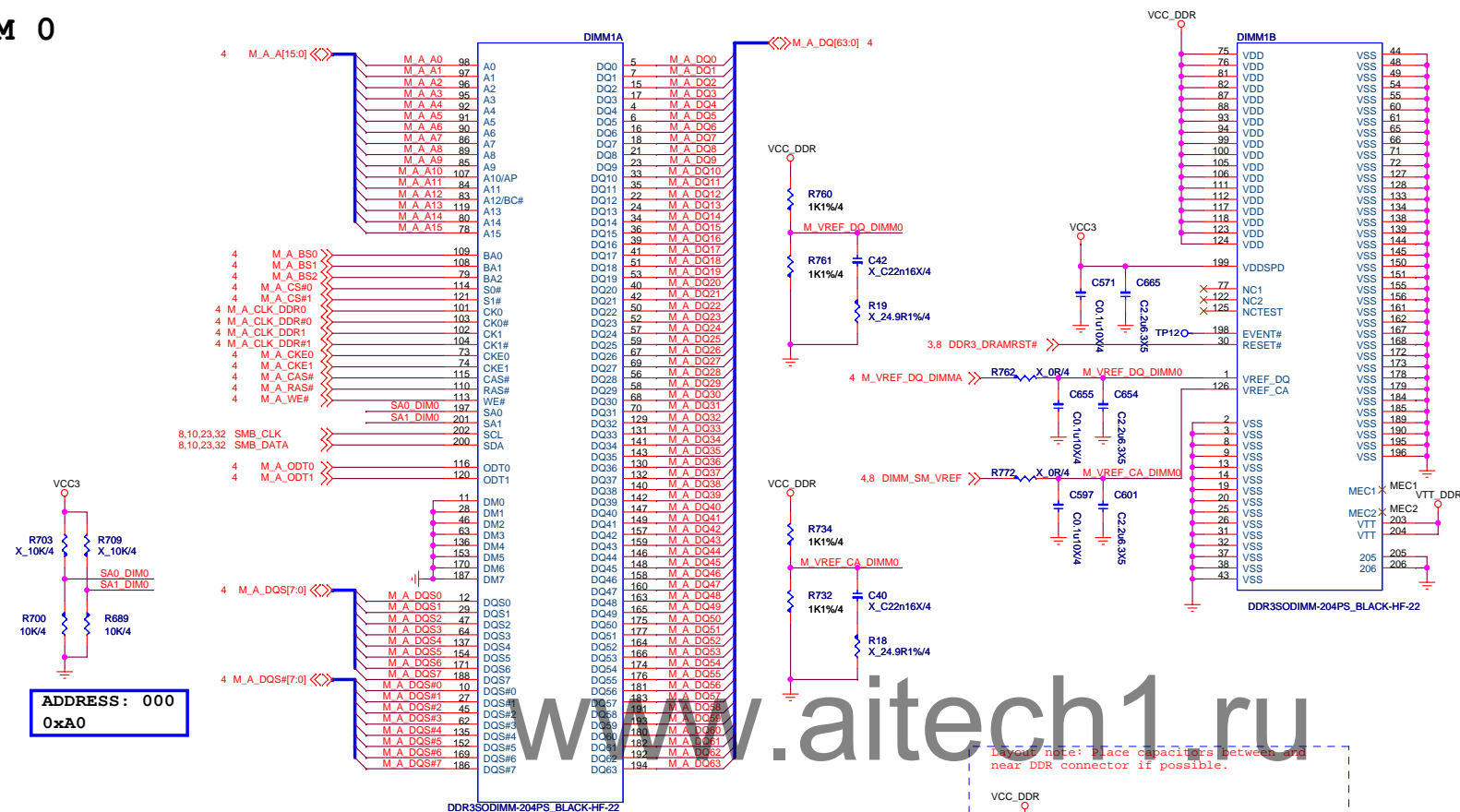
eDP Enable

PCI Express\* Bifurcation

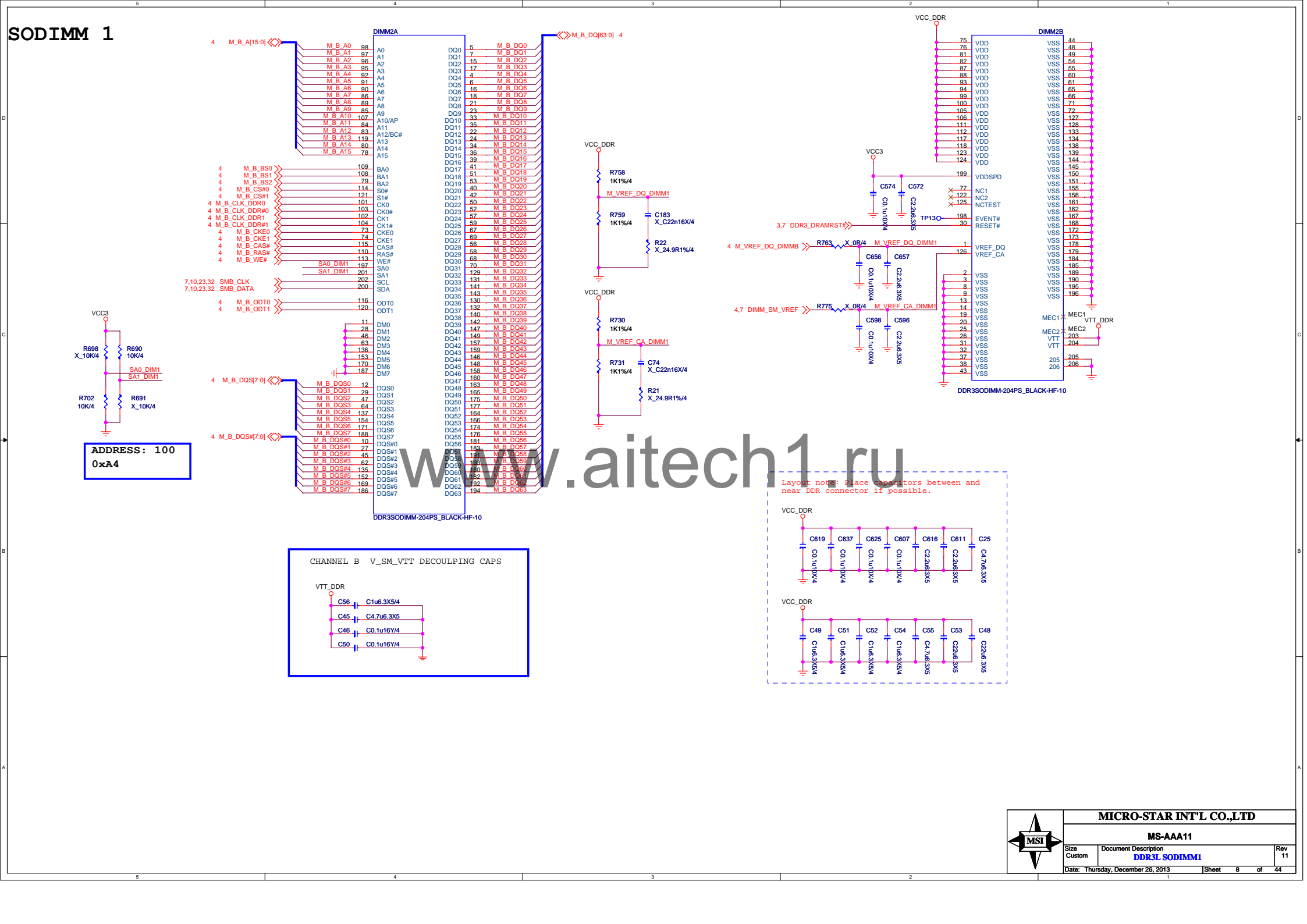
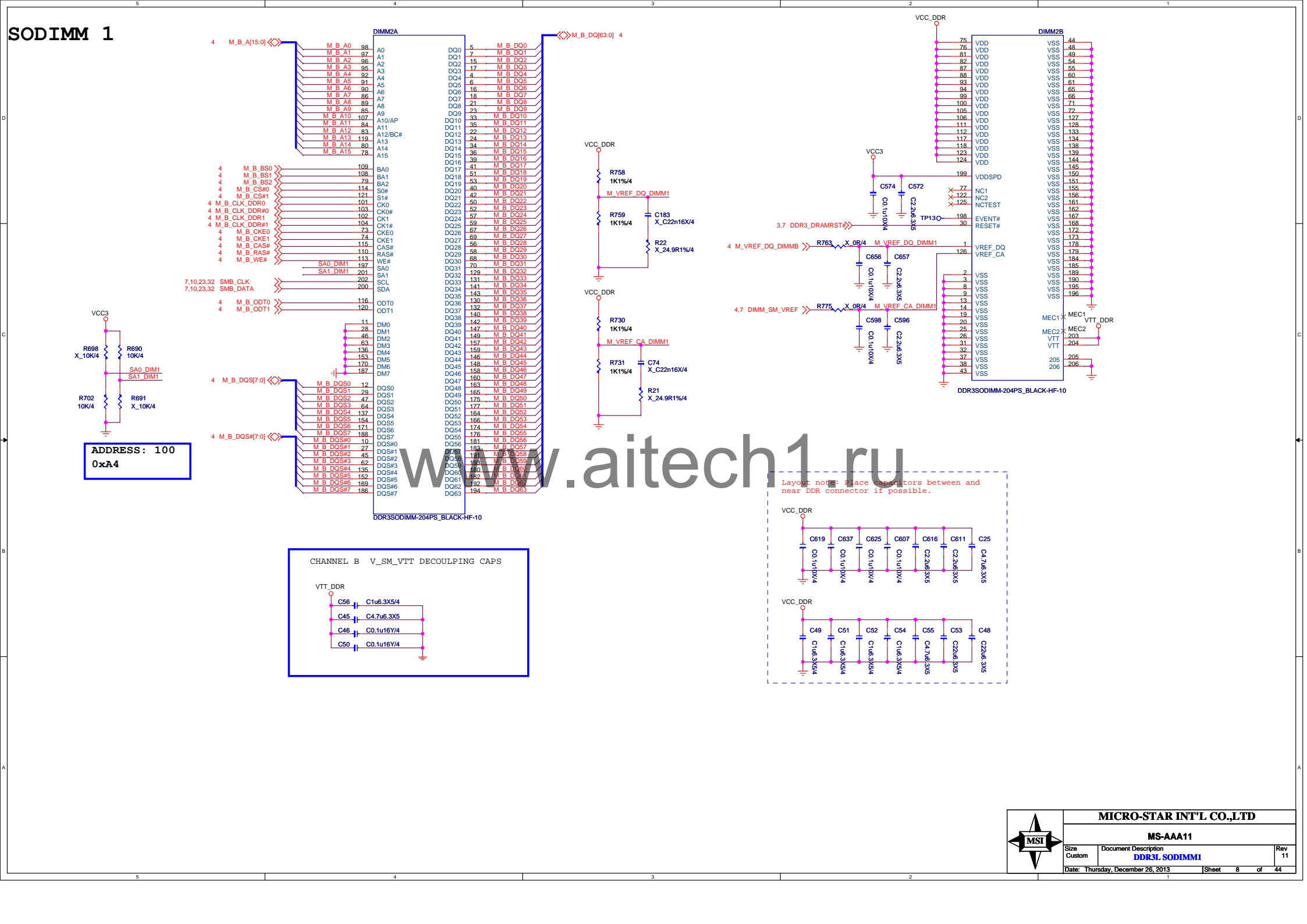
PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
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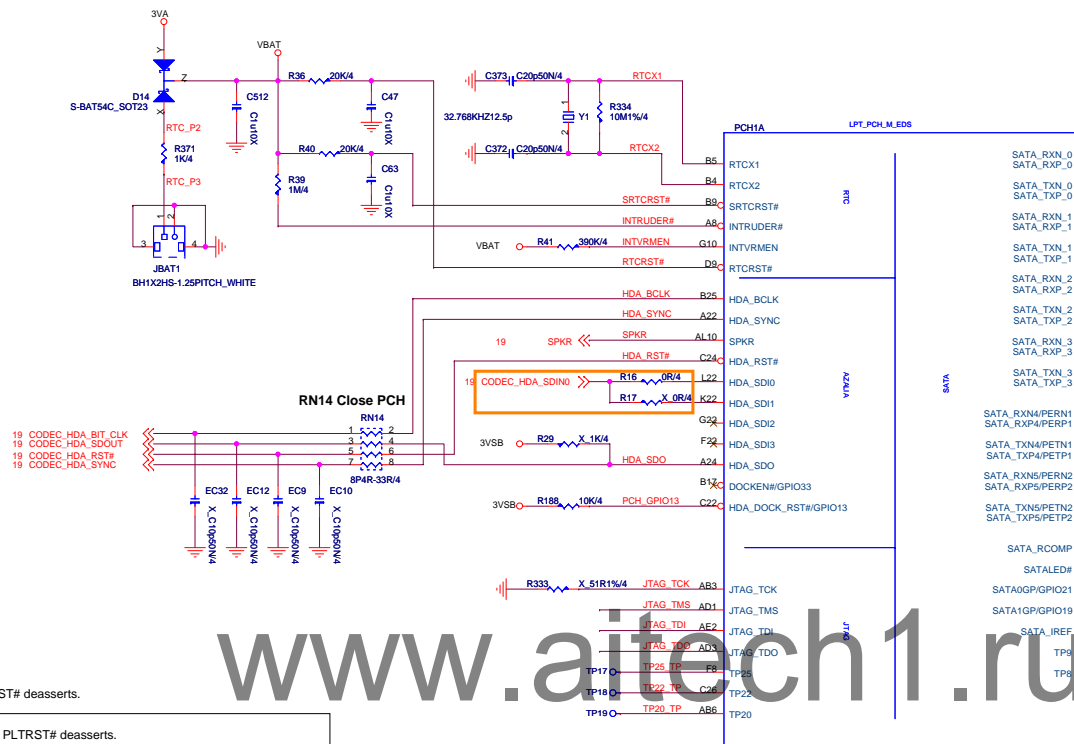
# SODIMM 0



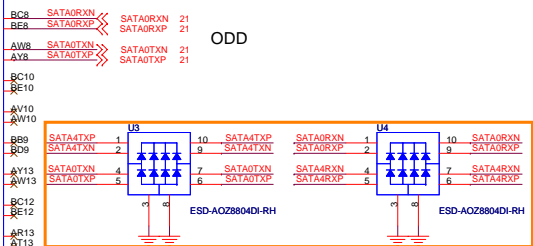
Layout note: Place capacitors between and near DDR connector if possible.

[illegible]





SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
QM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A



SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
QM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

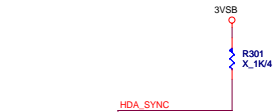
SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
QM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

Flash Descriptor Security Protect		
HDA_SDO	Low = Enable	High = Disable

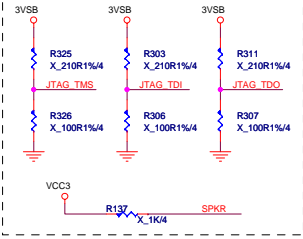
Signal has a weak internal pull-down  
Note: The weak internal pull-down is disabled after PLTRST# deasserts.

SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
QM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

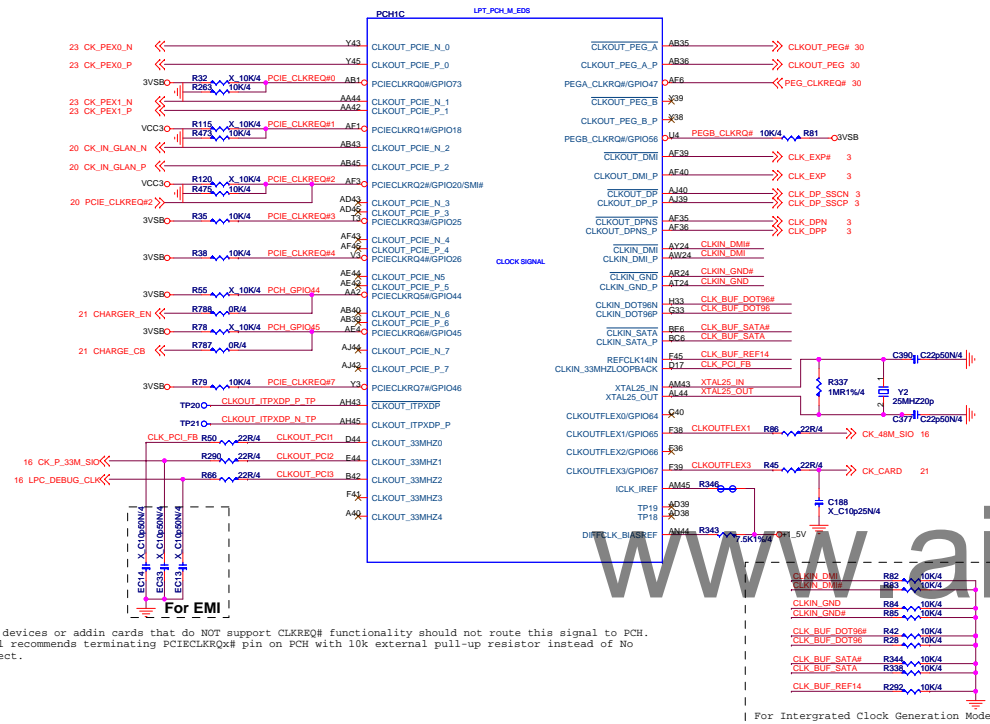
Reserved for Codec use RUN.



HDA\_SYNC signal also serves as a strap for selecting VRM voltage to the PCH.  
The strap is sampled on the rising edge of RSMRST# signal.  
Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input.  
Therefore, platform may need to isolate this signal from the codec during the strap phase. The following example circuits maybe used to achieve this purpose.

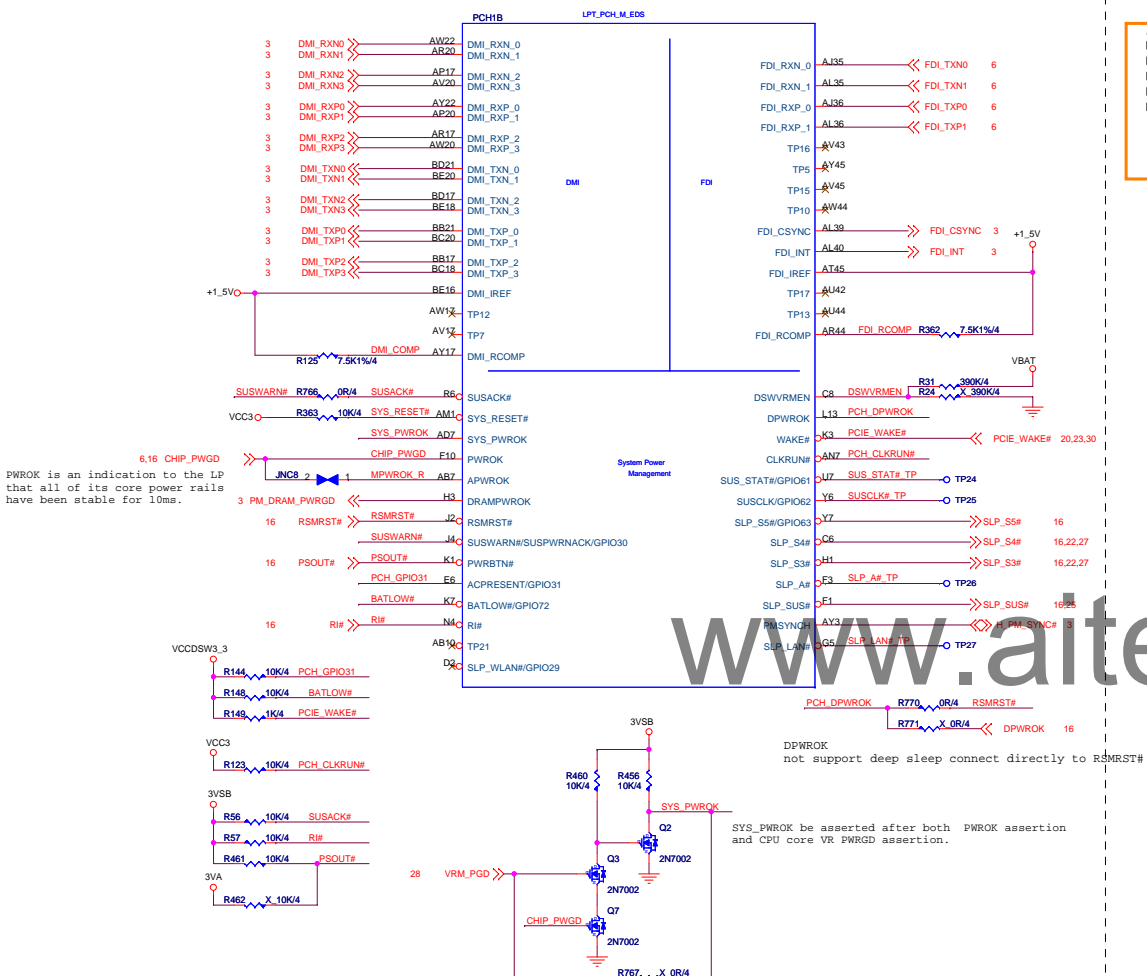


Only PCIECLKRQ[2:1]# on PCH  
are core well powered. All other  
PCIECLKRQx# are suspend well powered.  
---Checklist

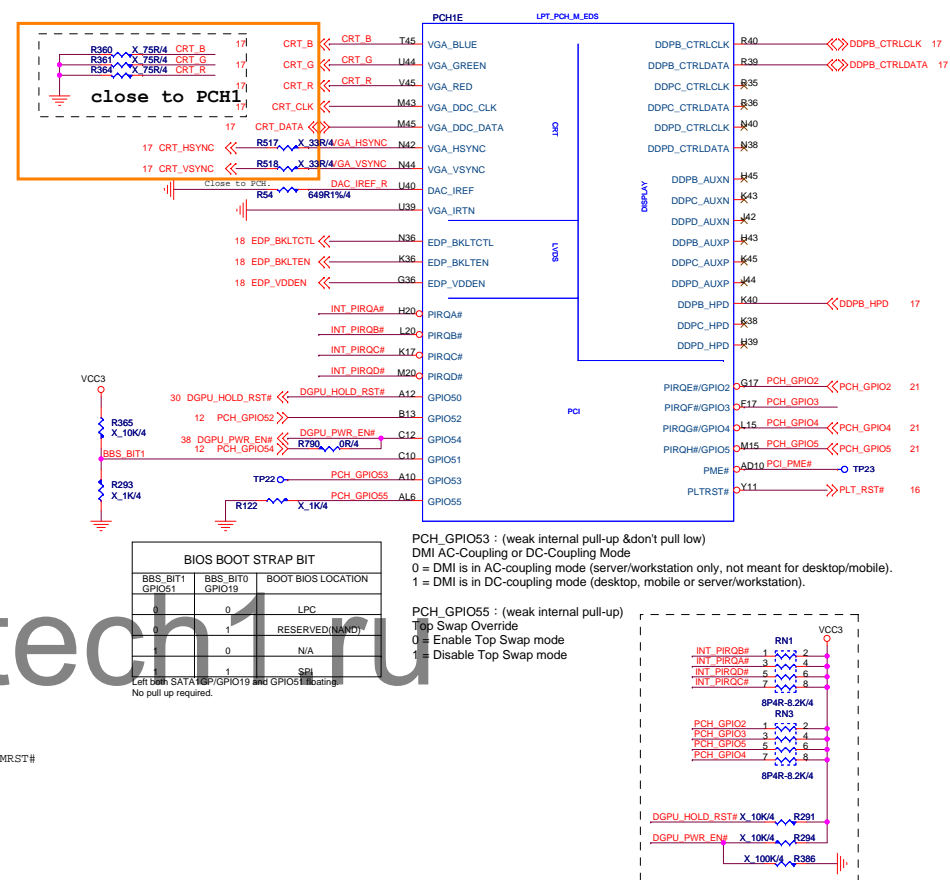


| For Intergrated Clock Generation Mode

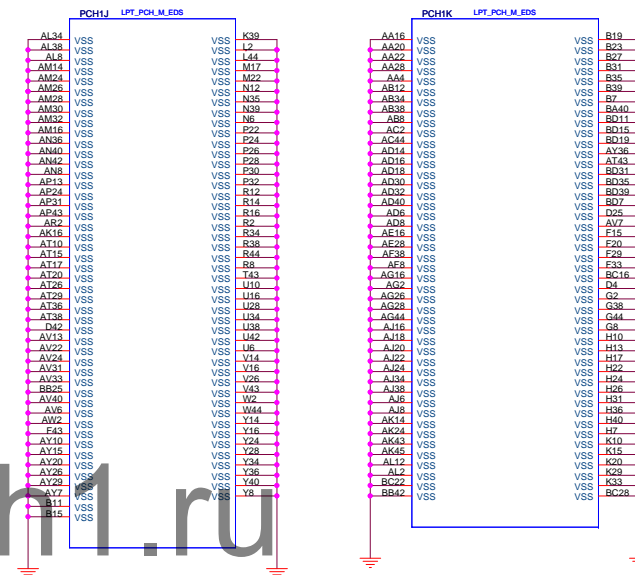
## Lynx Point (DMI, FDI)



## Lynx Point (PCI, DDI)



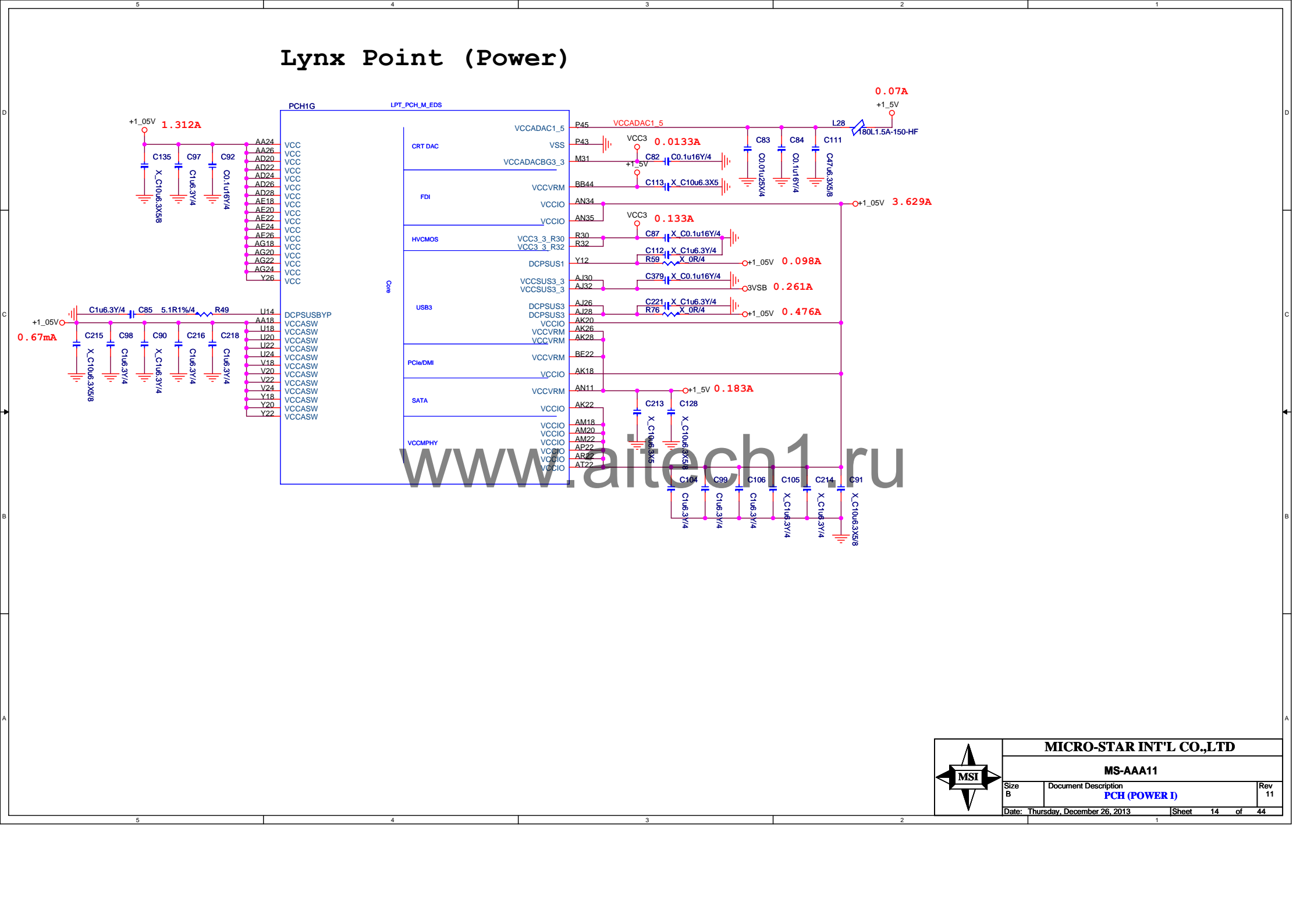
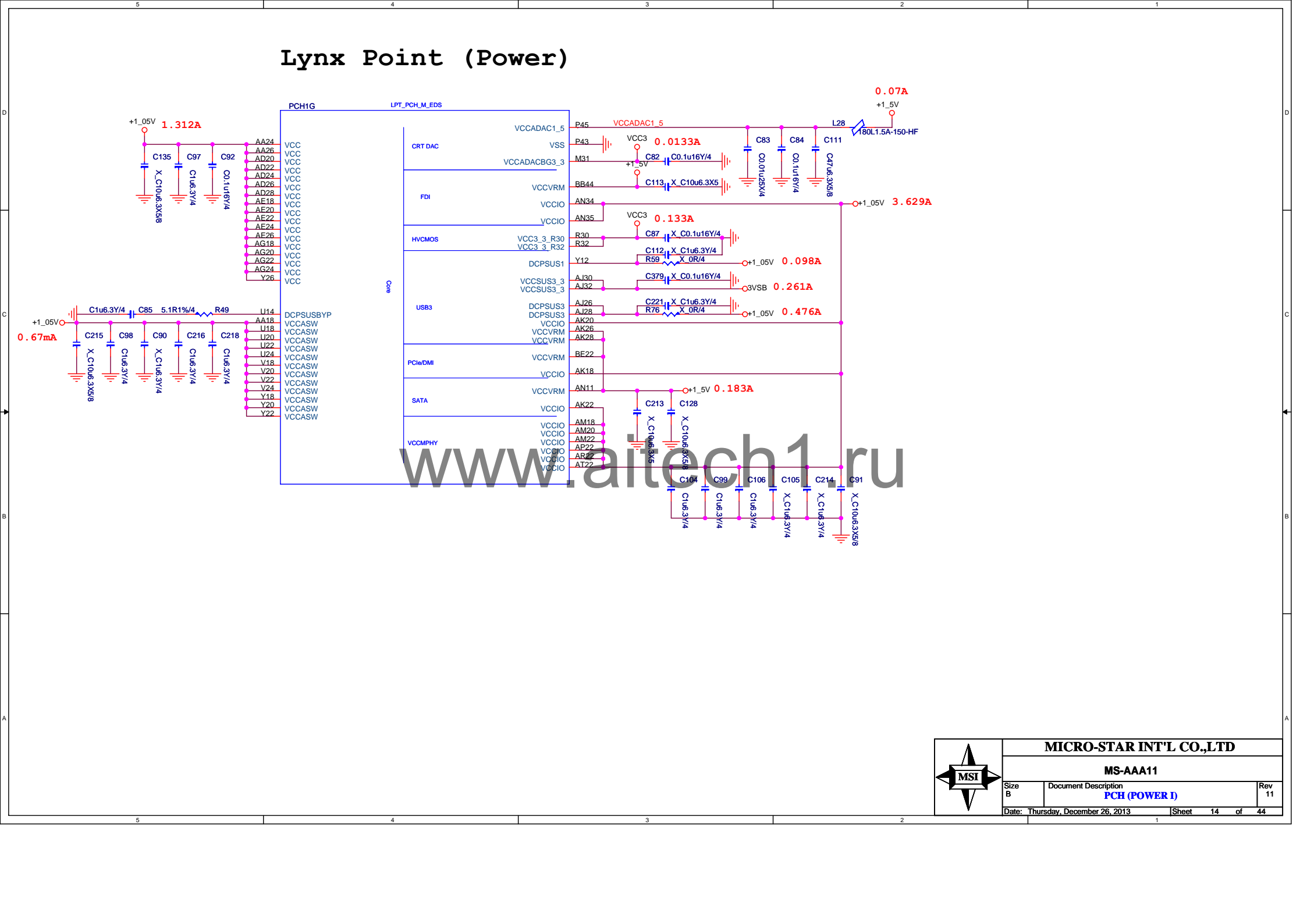
Lynx Point (Gnd)

[illegible]

# Lynx Point (PCIE,USB)



SKU	USB3-1	USB3-2	USB3-3	USB3-4	USB3-5	USB3-6
QM87	O	O	O	O	O	O
HM87	O	O	O	O	O	O
HM86	O	O	O	O	X	X

[illegible]

# Lynx Point (Power)

The schematic illustrates the power distribution for the Lynx Point system, centered around the LPT\_PCH\_M\_EDS block. It shows the following power rails and their associated components and current loads:

- +1.05V Rail:** Sourced from a 1.312A input, it branches into several sub-rails:
  - VCC/VSS:** Connected to pins AA24, AA26, AD22, AD24, AD26, AD28, AE18, AE20, AE22, AE24, AE26, AG18, AG20, AG22, AG24, and Y26.
  - VCCADAC1\_5:** Connected to P45, with a current load of 0.0133A.
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail:** Sourced from a 0.07A input, it branches into:
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail (3.629A):** Sourced from a 3.629A input, it branches into:
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail (0.098A):** Sourced from a 0.098A input, it branches into:
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail (0.261A):** Sourced from a 0.261A input, it branches into:
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail (0.476A):** Sourced from a 0.476A input, it branches into:
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail (0.183A):** Sourced from a 0.183A input, it branches into:
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins U14, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPCV:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.

[illegible][illegible]

# Lynx Point (Power)

The schematic illustrates the power distribution for the Lynx Point system, centered around the LPT\_PCH\_M\_EDS block. It shows the following power rails and their associated components and current loads:

- +1.05V Rail:** Sourced from a 1.312A input, it branches into several sub-rails:
  - VCC/VSS:** Connected to pins AA24, AA26, AD22, AD24, AD26, AD28, AE18, AE20, AE22, AE24, AE26, AG18, AG20, AG22, AG24, and Y26.
  - VCCADAC1\_5:** Connected to P45, with a current load of 0.0133A.
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins AA18, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPHY:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.5V Rail:** Sourced from a 0.07A input, it branches into:
  - VCCADAC1\_5:** Connected to P45, with a current load of 0.0133A.
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins AA18, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPHY:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.
- +1.05V Rail (0.67mA):** Sourced from a 0.67mA input, it branches into:
  - VCC/VSS:** Connected to pins AA24, AA26, AD22, AD24, AD26, AD28, AE18, AE20, AE22, AE24, AE26, AG18, AG20, AG22, AG24, and Y26.
  - VCCADAC1\_5:** Connected to P45, with a current load of 0.0133A.
  - VCC3:** Connected to AN34 and AN35, with a current load of 0.133A.
  - VCC3\_3\_R30:** Connected to R30 and R32.
  - VCC3\_3\_R32:** Connected to R32.
  - VCCVRM:** Connected to BB44, BB46, and BB48.
  - VCCIO:** Connected to AN34, AN35, AK18, and AK22.
  - VCCASW:** Connected to pins AA18, U18, U20, U22, U24, V18, V20, V22, Y18, Y20, and Y22.
  - VCCMPHY:** Connected to pins AM18, AM20, AM22, AP22, AR22, and AT22.

The schematic also shows various capacitors (C135, C97, C92, C106, C104, C93, C106, C105, C214, C91) and resistors (R49, R59, R76, R30, R32) used for decoupling and signal conditioning. A large watermark 'www.aitech1.ru' is visible across the center of the diagram.

MICRO-STAR INT'L CO.,LTD		
MS-AAA11		
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PCH (POWER I)		
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[illegible]

# Lynx Point (Power)

The schematic illustrates the power distribution for the Lynx Point system, centered around the LPT\_PCH\_M\_EDS block. It shows the following power rails and their associated components and current loads:

- +1.05V Rail:** Supplies power to the PCH1G block (1.312A) and the DCPSUSBYP block (0.67mA). It also feeds the VCC3 rail through a 0.0133A load.
- VCC3 Rail:** A central 1.5V rail that branches into several other rails:
  - VCC3\_3\_R30:** 0.133A
  - VCC3\_3\_R32:** 0.133A
  - VCC3\_3\_R32:** 0.098A
  - VCC3\_3\_R32:** 0.261A
  - VCC3\_3\_R32:** 0.476A
  - VCC3\_3\_R32:** 0.183A
- VCC3\_3\_R32 Rail:** 0.07A
- VCC3\_3\_R32 Rail:** 3.629A
- VCC3\_3\_R32 Rail:** 0.07A

The schematic also shows the connection of various components to these rails, including capacitors (C135, C97, C92, C106, C104, C99, C106, C105, C214, C91, C104, C99, C106, C105, C214, C91), resistors (R59, R76, R49), and integrated circuits (U14, U18, U20, U22, U24, V18, V20, V22, Y24, Y18, Y20, Y22).

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# Lynx Point (Power)

The schematic illustrates the power distribution for the Lynx Point system. It features several main power rails and their associated components:

- +1.05V Rail:** Supplied by a 1.312A source, this rail feeds various components including the CRT DAC, FDI, HVC MOS, USB3, PCIe/DMI, SATA, and VCCMPHY. It includes components like C135, C97, C92, C0.1u6V/4, C1u6.3Y/4, C85, 5.1R1%/4, R49, U14, AA18, U18, U20, U22, U24, V18, V20, V22, Y24, Y18, Y20, and Y22.
- +1.5V Rail:** Supplied by a 0.07A source, this rail feeds the VCCADAC1\_5 and VCC3 rails. It includes components like C82, C0.1u16Y/4, C0.01u25X/4, C83, C84, C111, C47u6.3X/5/8, and L28 (180L1.5A-150-HF).
- +3.3V Rail:** Supplied by a 3.629A source, this rail feeds the VCC3\_3\_R30 and VCC3\_3\_R32 rails. It includes components like C87, C0.1u16Y/4, C112, C1u6.3Y/4, R59, X 0R/4, C379, C0.1u16Y/4, C221, C1u6.3Y/4, R76, X 0R/4, and C213.
- +0.9V Rail:** Supplied by a 0.098A source, this rail feeds the VCC3\_3\_R30 and VCC3\_3\_R32 rails. It includes components like C87, C0.1u16Y/4, C112, C1u6.3Y/4, R59, X 0R/4, C379, C0.1u16Y/4, C221, C1u6.3Y/4, R76, X 0R/4, and C213.
- +0.6V Rail:** Supplied by a 0.67mA source, this rail feeds the VCC3\_3\_R30 and VCC3\_3\_R32 rails. It includes components like C87, C0.1u16Y/4, C112, C1u6.3Y/4, R59, X 0R/4, C379, C0.1u16Y/4, C221, C1u6.3Y/4, R76, X 0R/4, and C213.

The schematic also shows the connection of various components to the power rails, including the CRT DAC, FDI, HVC MOS, USB3, PCIe/DMI, SATA, and VCCMPHY. The current measurements are provided for each main rail.

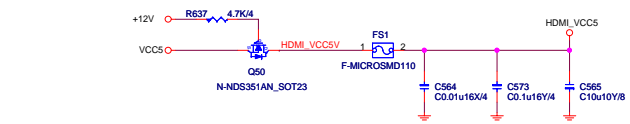
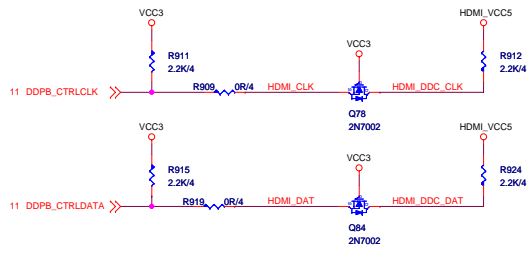
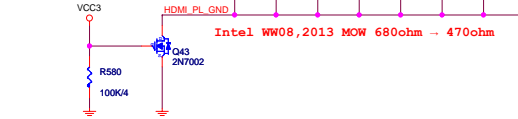
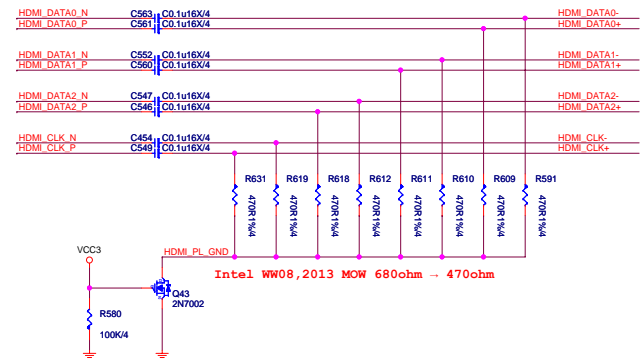
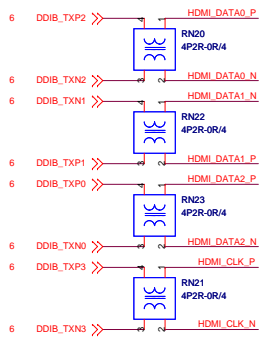
Size	Document Description	Rev
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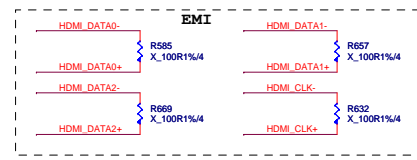
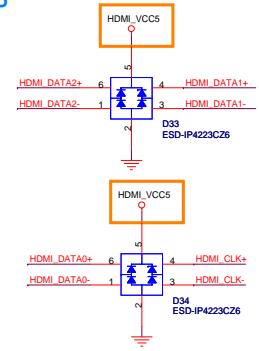
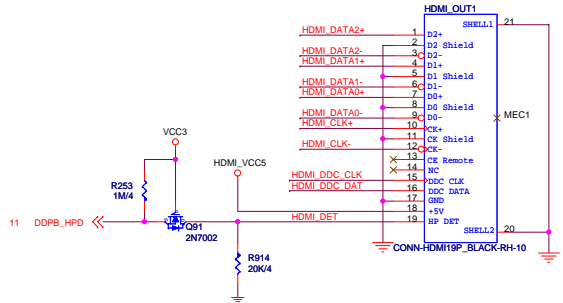




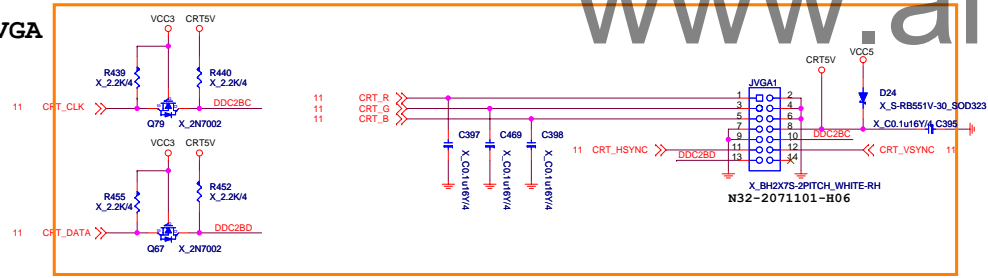




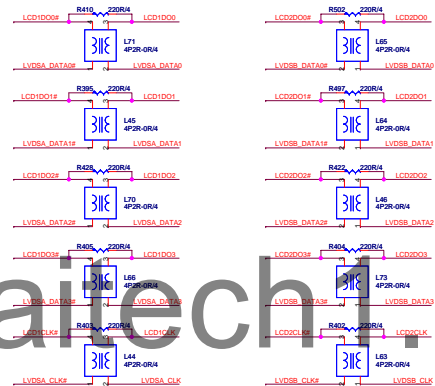
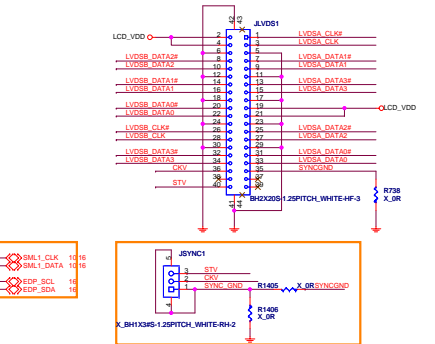
# N5I-19M0161-L06



## VGA

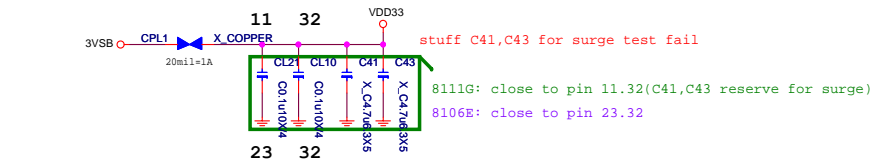
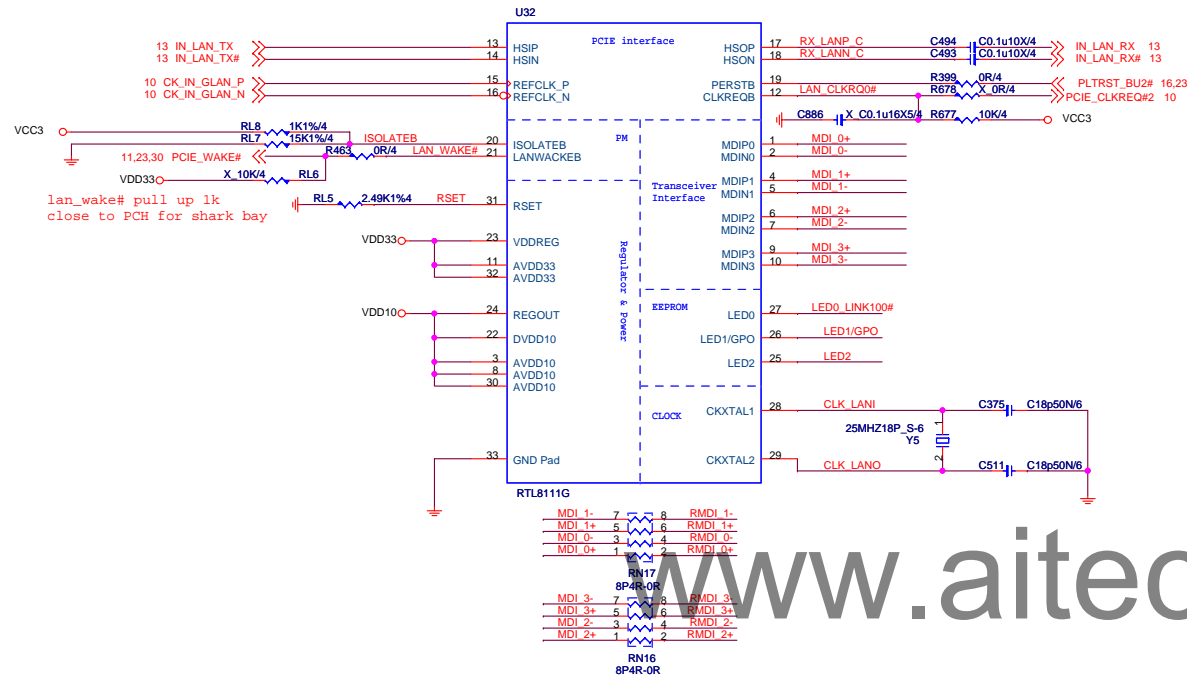


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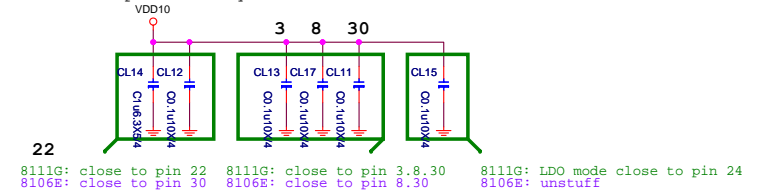




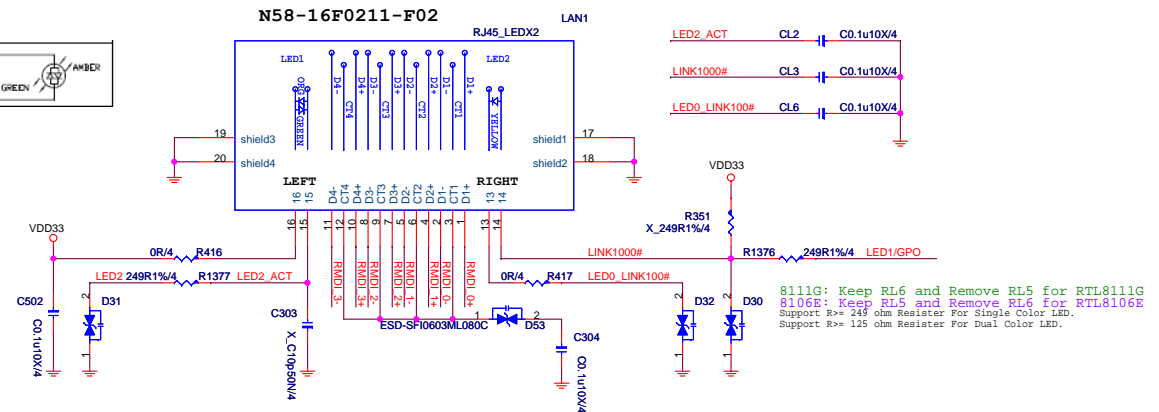
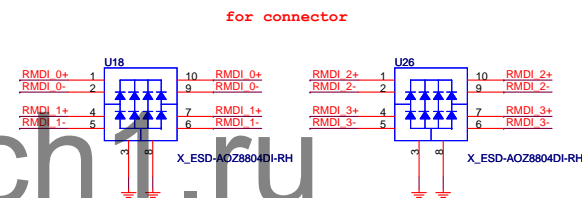
RTL8111G Giga LAN  
RTL8106E 10/100M LAN



Icc33 average operating supply current from 3.3V  
At 1Gbps with heavy network traffic 70mA



30 Icc10 average operating supply current from 1.0V  
At 1Gbps with heavy network traffic 300mA



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MS-AAA11

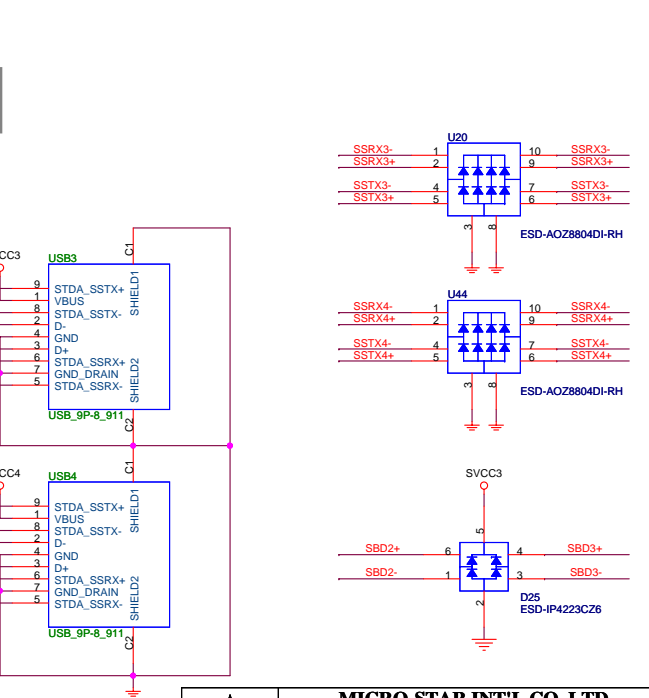
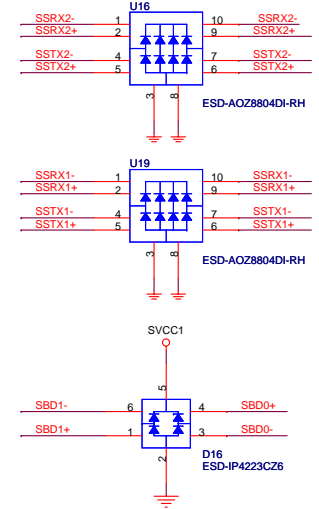
Size Custom	Document Description <b>LAN-RTL8111G</b>
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Date: Thursday, December 26, 2013 Sheet 20 of 44

Rev  
11



### POWER CIRCUIT FOR USB3.0 PORT3&4



Size Custom	Document Description <b>USB 3.0 Port</b>	Rev 11
Date: Thursday, December 26, 2013		Sheet 22 of 44



19V TO 12V

$$I_{ripple} = 2.7A$$

$$2 * 2.8 * 0.9 = 5.04A > 2.7A$$

5.5A

Trace list for layout==>Width:25 , Spacing:20

HG\_R\_U11  
PHASE\_R\_U11  
LG\_U11



MICRO-STAR INT'L CO.,LTD

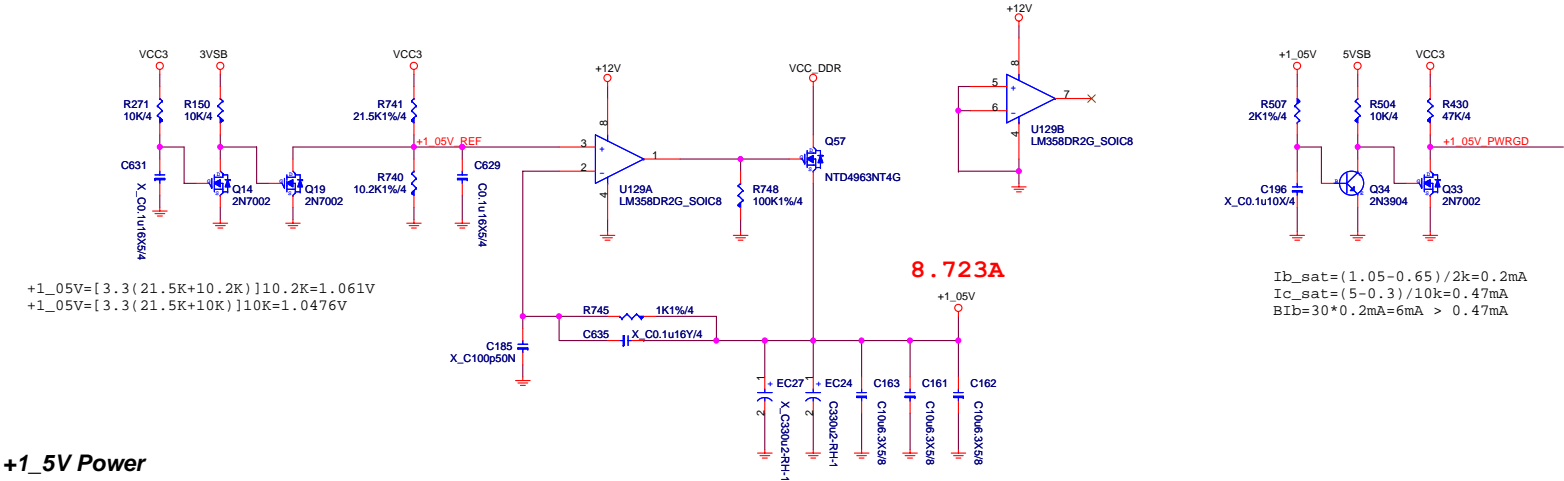
MS-AAA11

Size	Document Description	Rev
B	DC_IN/+12V	11
Date: Thursday, December 26, 2013 Sheet 24 of 44		

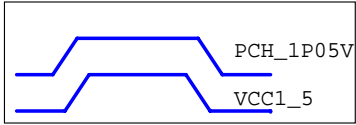


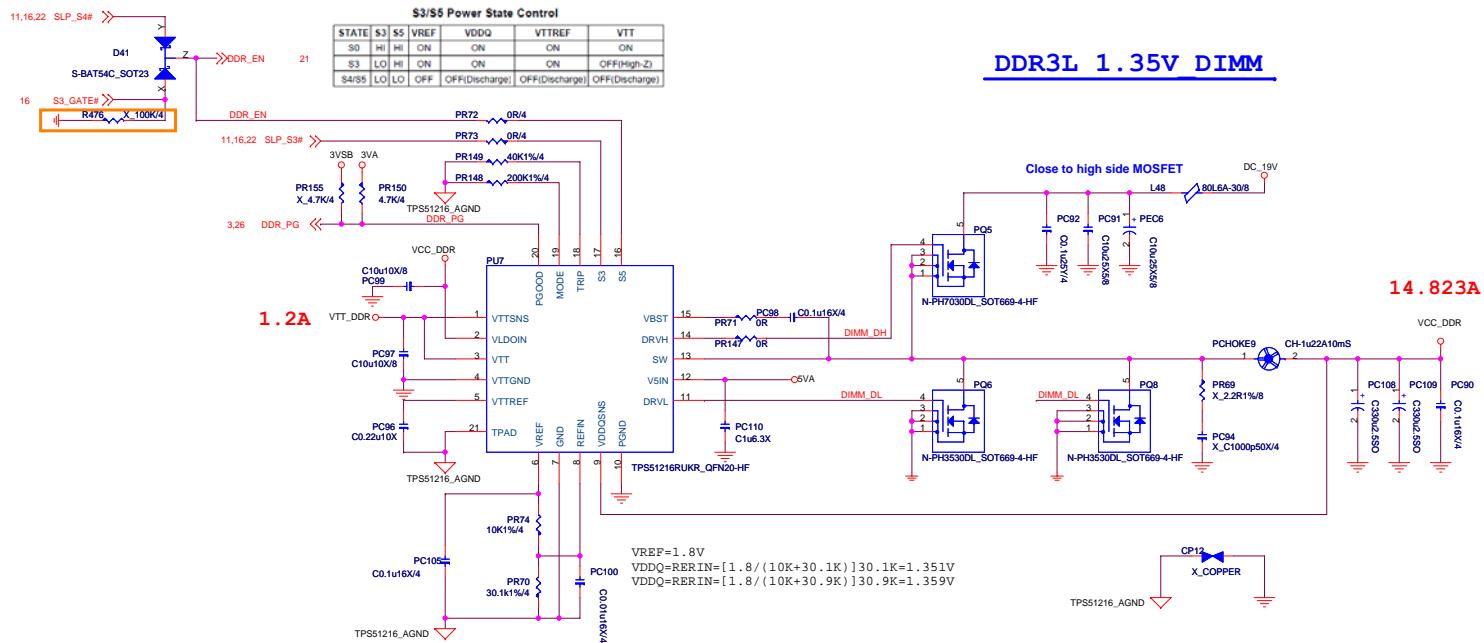


**+1\_05V Power**



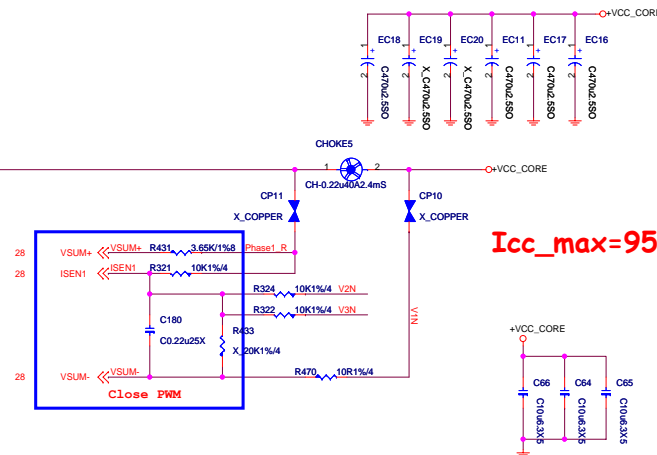
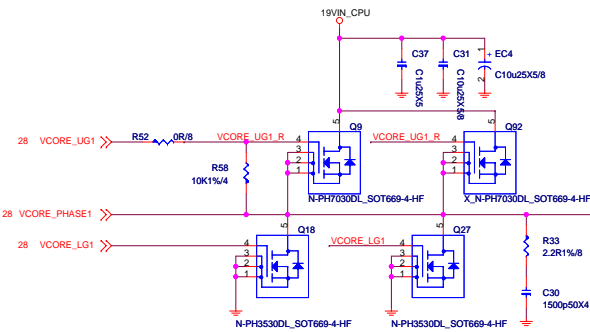
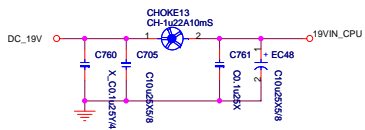
**+1\_5V Power**



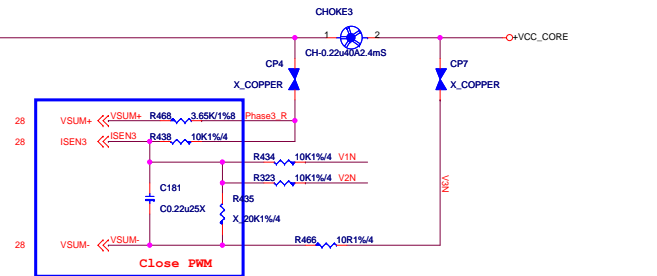
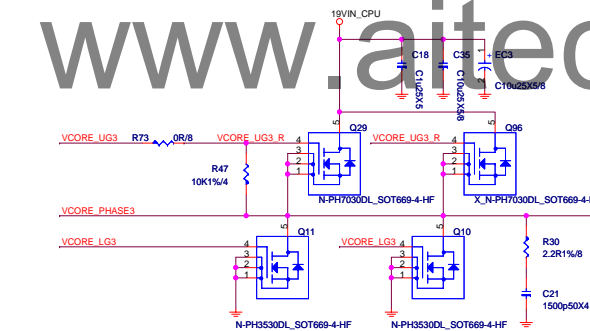
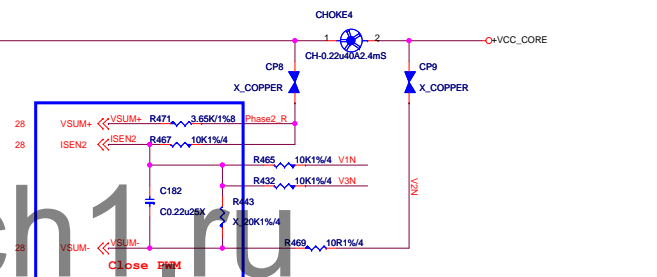
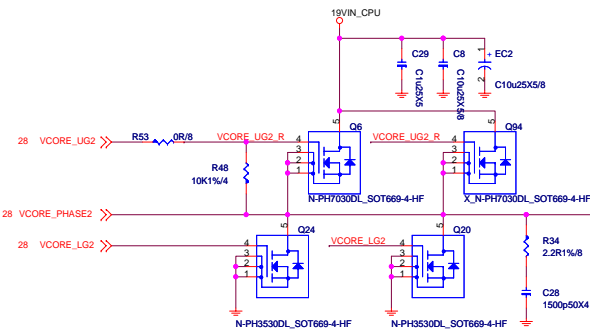


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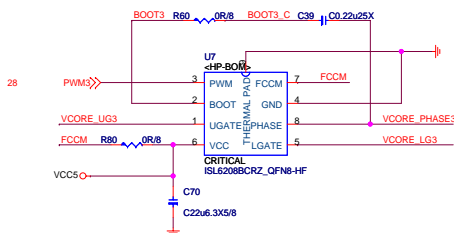




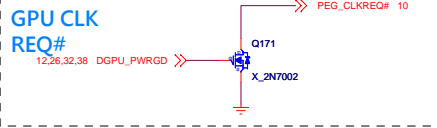
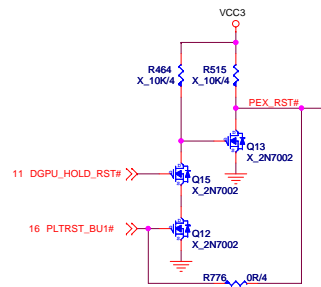
**Icc\_max=95A**



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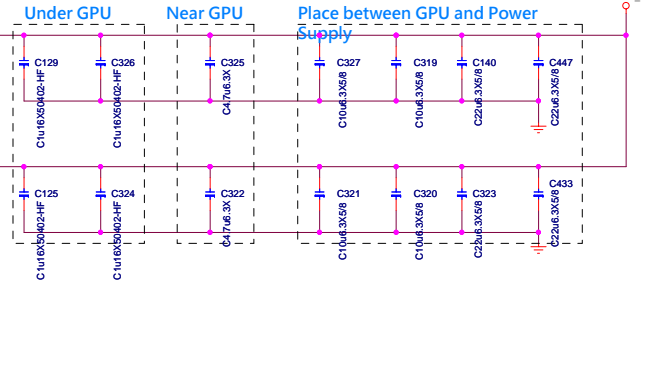


# N14M-GE( PCI-Express Gen2 x8 Interface) N14P-GV2( PCI-Express Gen3 x8 Interface)



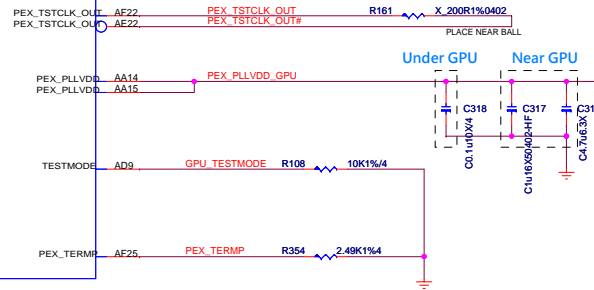
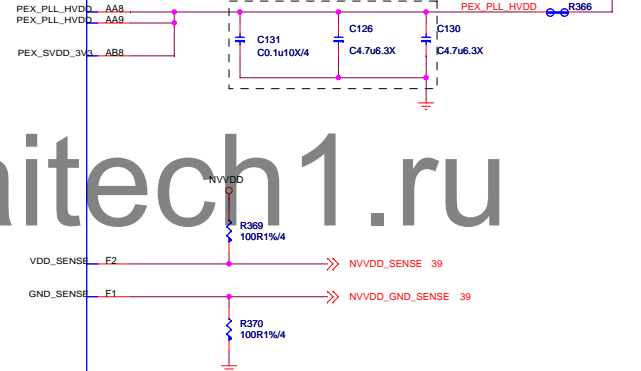
Design Guide Table14

4x 1u under GPU;  
2x 4.7u near GPU;  
4x 10u,4 x22u Place between GPU and Power Supply

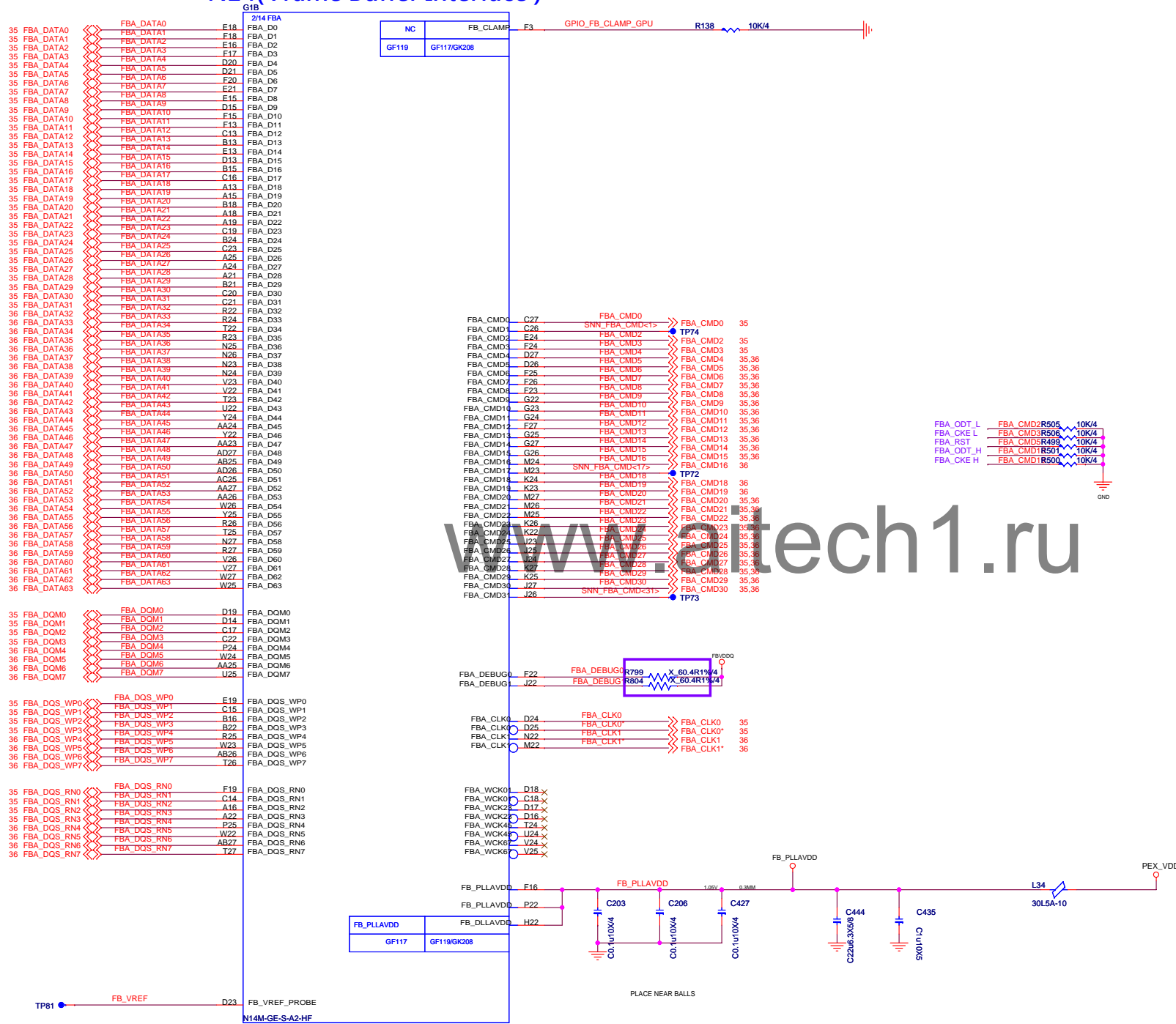


Design Guide Table16

1x 0.1u Near GPU;  
2x 4.7u Near GPU;  
Near GPU



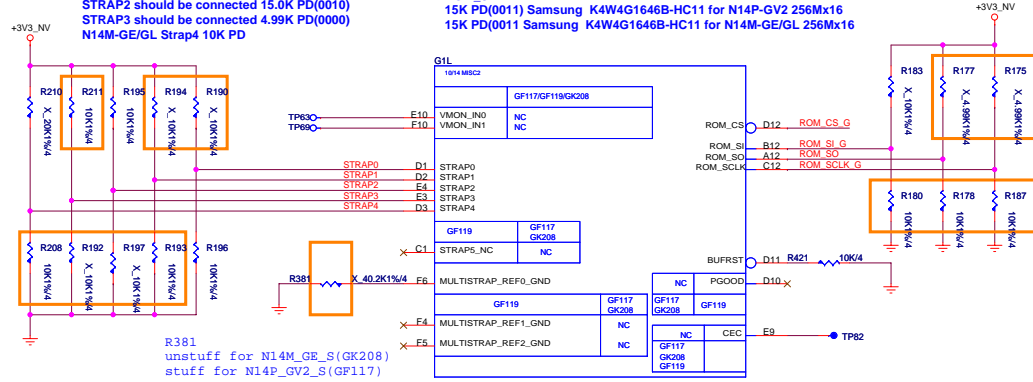
# N14( Frame Buffer Interface )



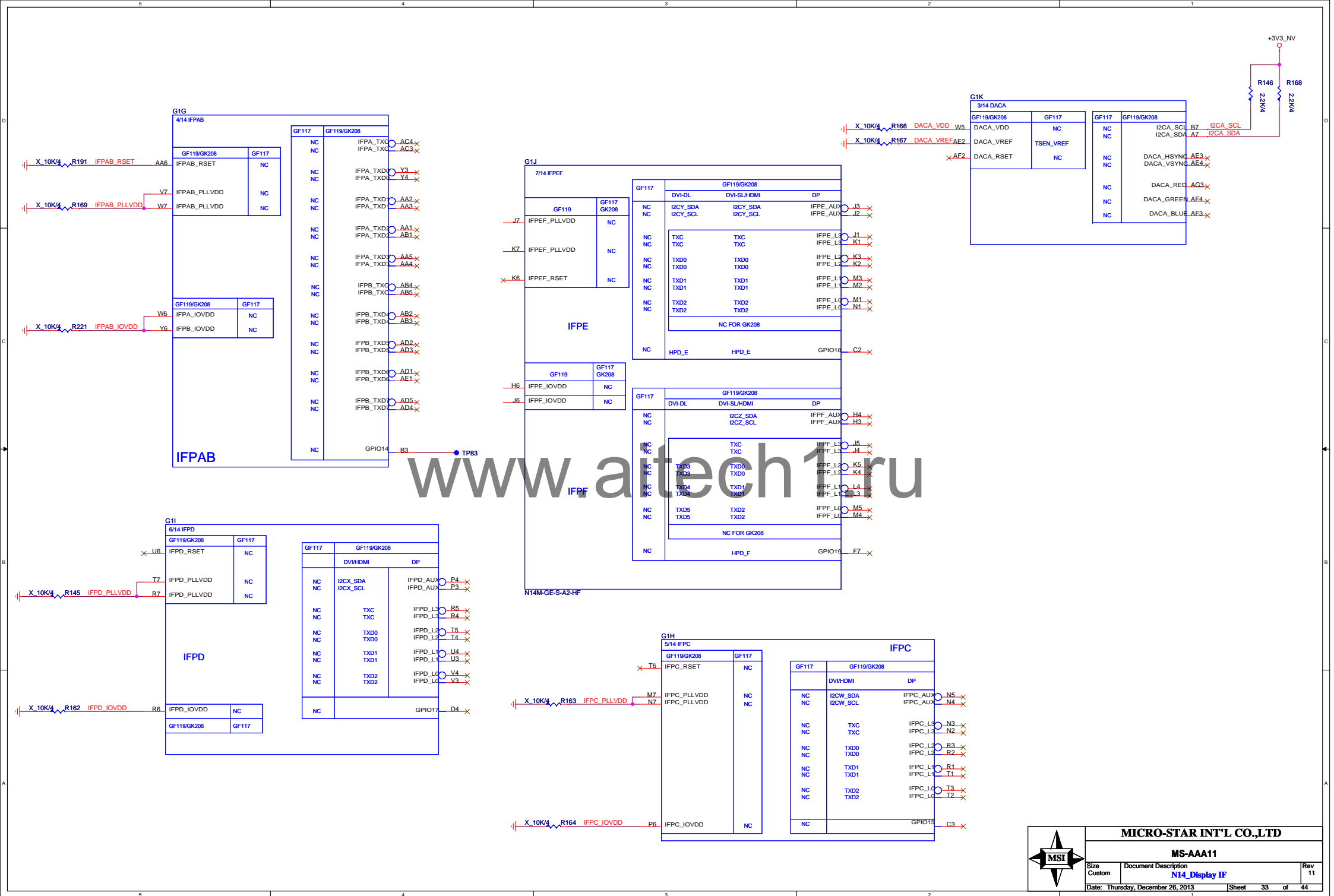
# N14M( Thermal & GPIO )

ROM\_SCLK:  
24.9K PU (1100) for N14P-GV2  
10K PD for N14M-GE/GL  
ROM\_SO:  
4.99K PU(1000) for N14P-GV2  
10K PD for N14M-GE/GL  
ROM\_SI:  
15K PD(0011) Samsung K4W4G1646B-HC11 for N14P-GV2 256Mx16  
15K PD(0011) Samsung K4W4G1646B-HC11 for N14M-GE/GL 256Mx16

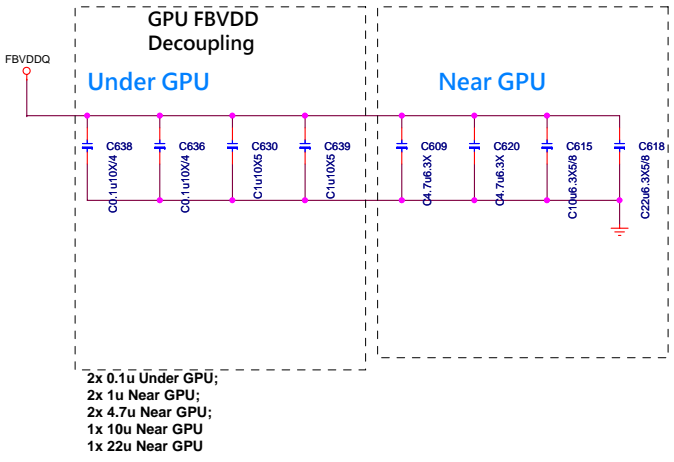
STRAP1 should be connected 45.3K PD(0111)  
STRAP2 should be connected 15.0K PD(0010)  
STRAP3 should be connected 4.99K PD(0000)  
N14M-GE/GL Strap4 10K PD



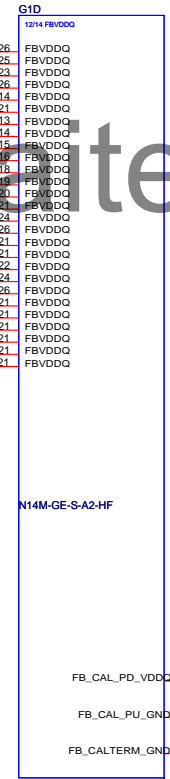
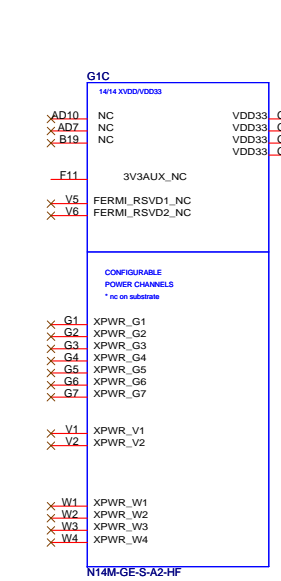
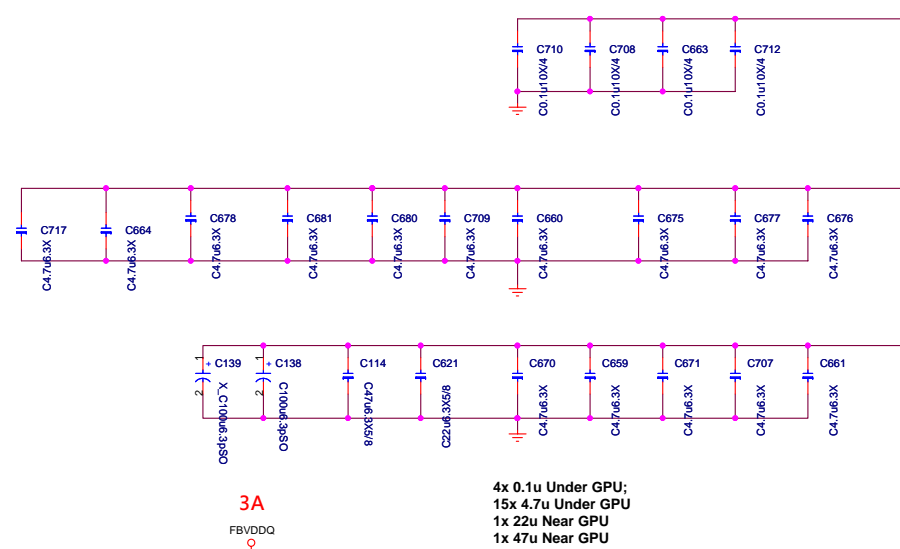




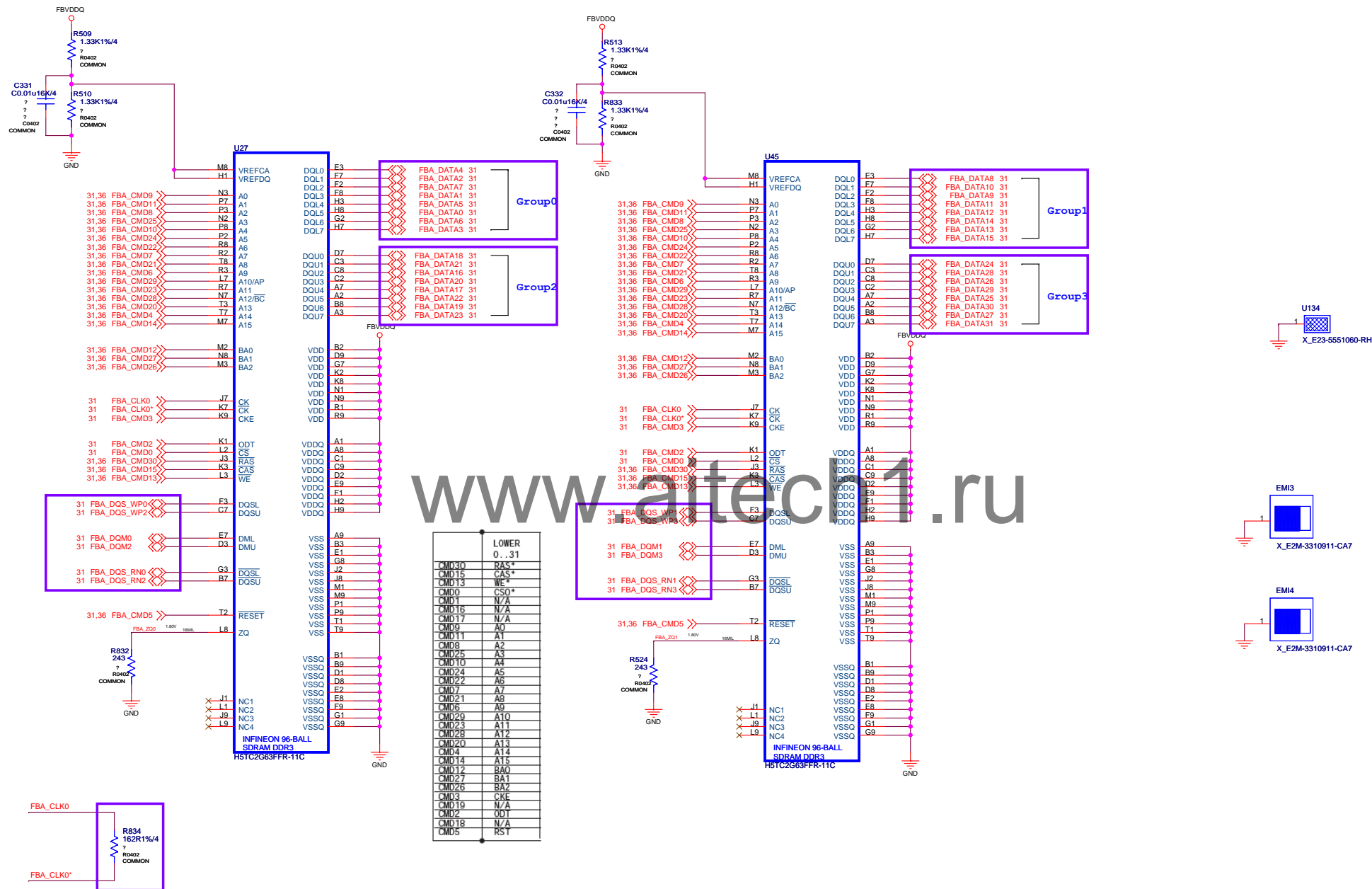
N14( Power & GND )



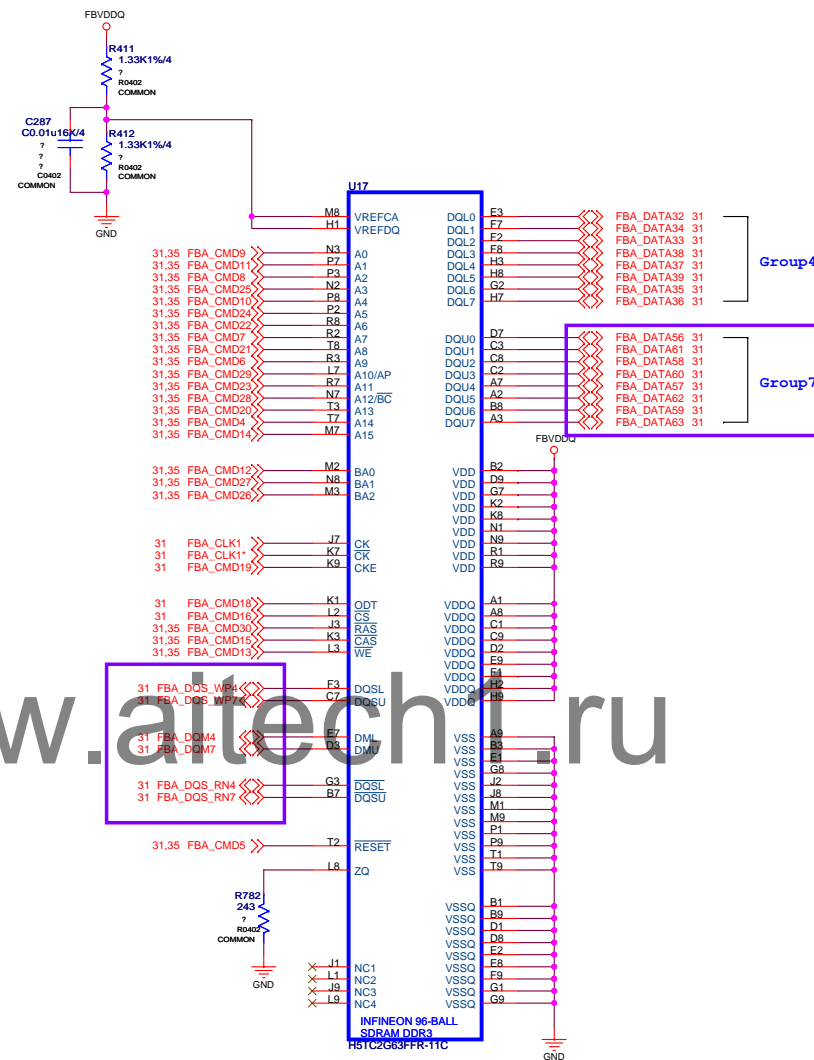
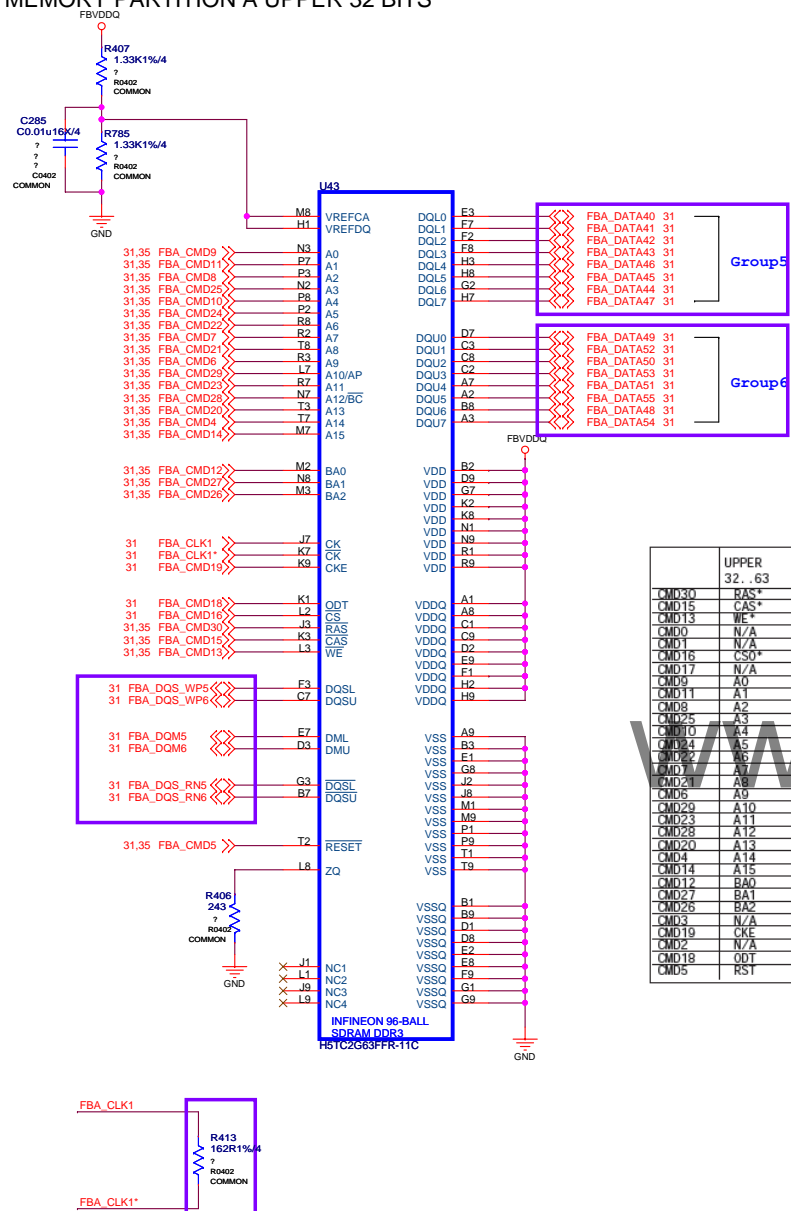
Under GPU



# MEMORY PARTITION A LOWER 32 BITS

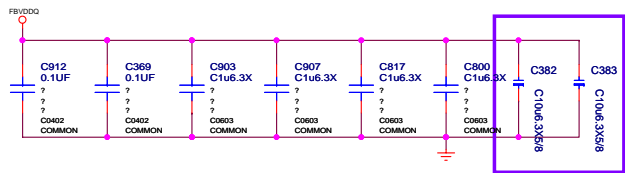


# MEMORY PARTITION A UPPER 32 BITS

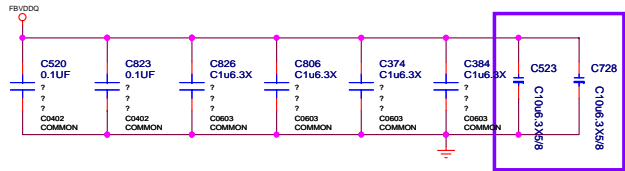


MEMORY DECOUPLING CAPS

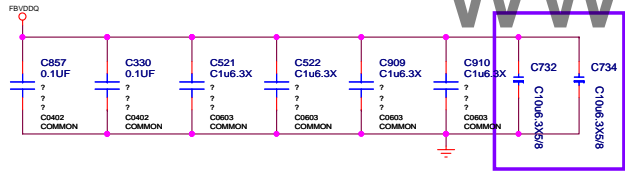
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



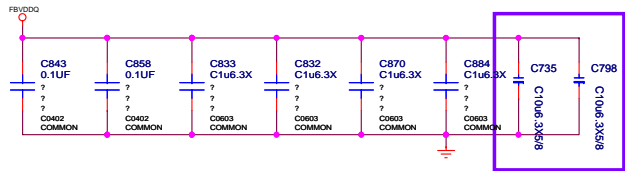
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



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# N14( Power Control )

EC Control DGPU\_PWR\_EN

EC Control NVVDD\_EN

DGPU\_PWM Control NVVDD\_PWERGD

+3VSUS

+3V3\_NV

NVVDD

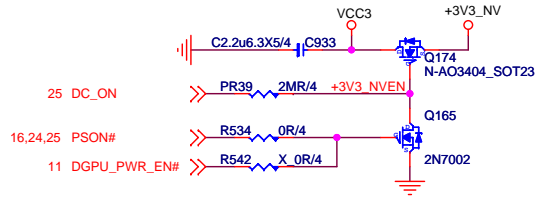
PEX\_VDD

DGPU\_PWRGD

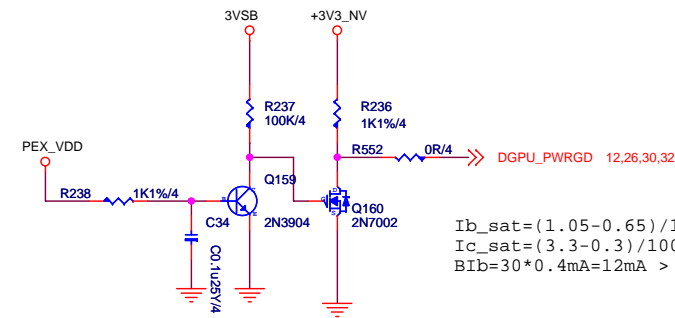
FBVDDQ

+3V3\_NV

0.295A



DGPU\_PWRGD



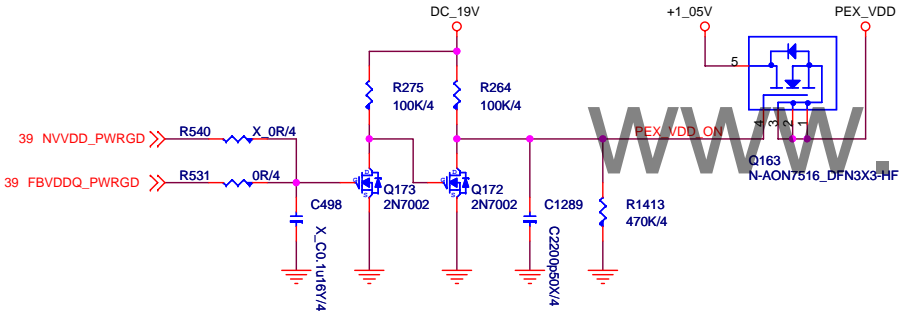
$$I_{b\_sat} = (1.05 - 0.65) / 1k = 0.4mA$$

$$I_{c\_sat} = (3.3 - 0.3) / 100k = 0.03mA$$

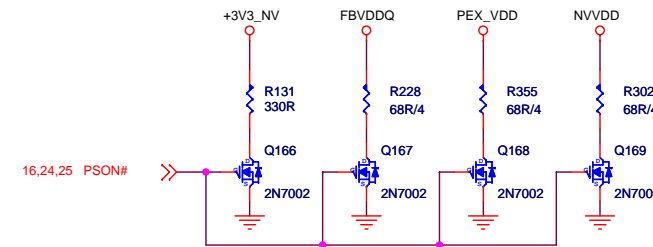
$$BIb = 30 * 0.4mA = 12mA > 0.03mA$$

PEX\_VDD

2.2A



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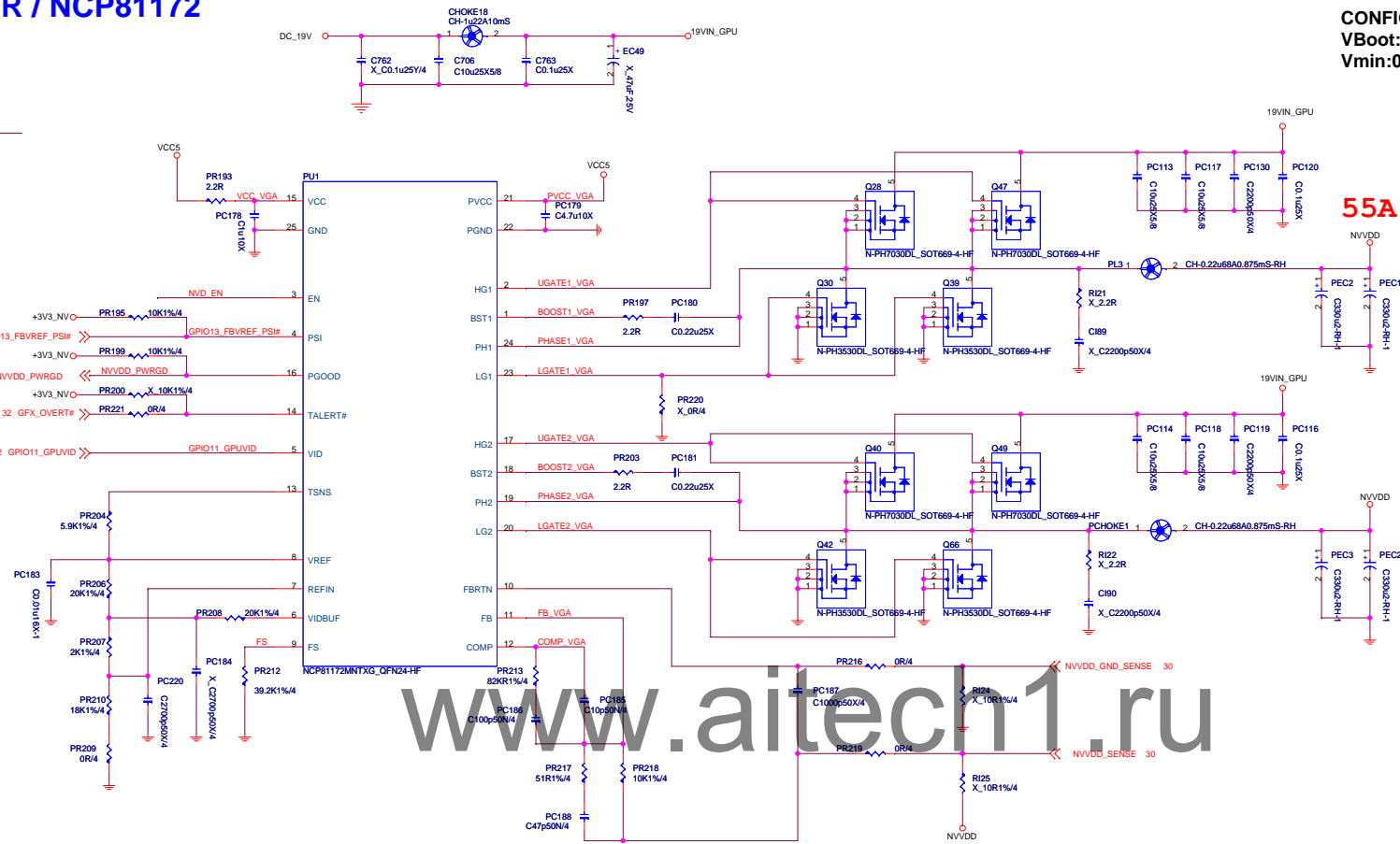
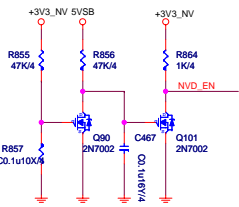
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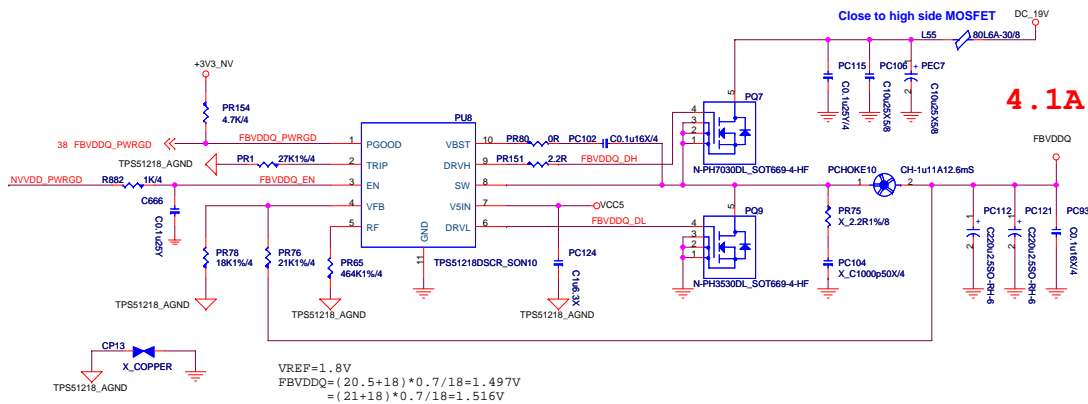
Size	Document Description	Rev
B	GPU_Power Control	11

Date: Thursday, December 26, 2013 Sheet 38 of 44

## NGPU POWER / NCP81172

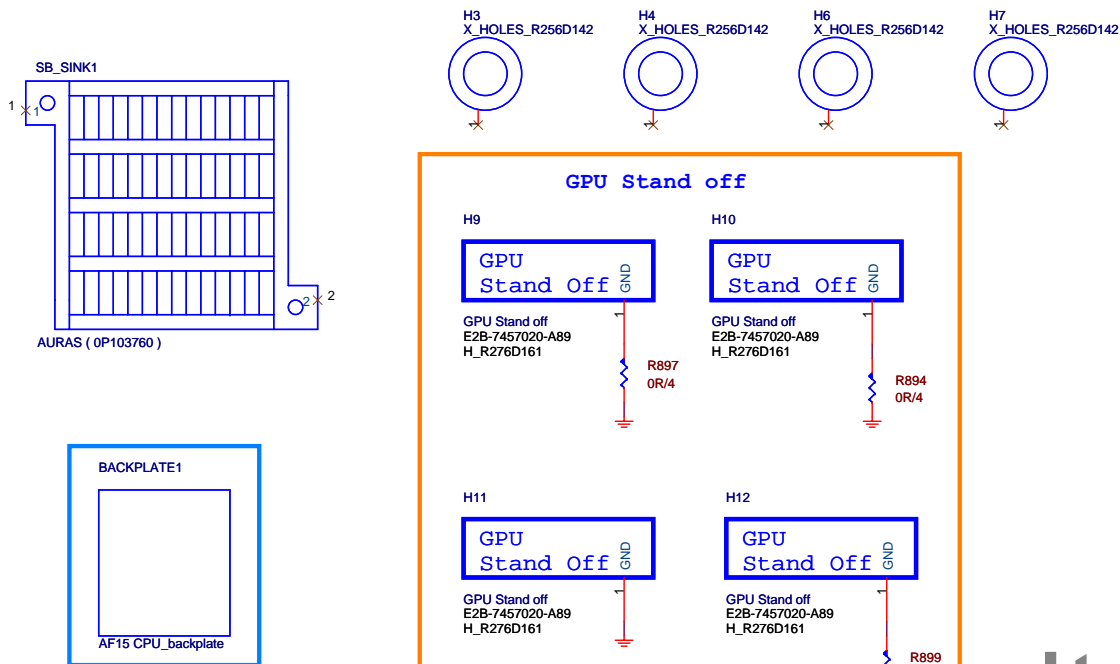


**CONFIG B**  
**VBoot:0.9V**  
**Vmin:0.6V / Vmax:1.2V**

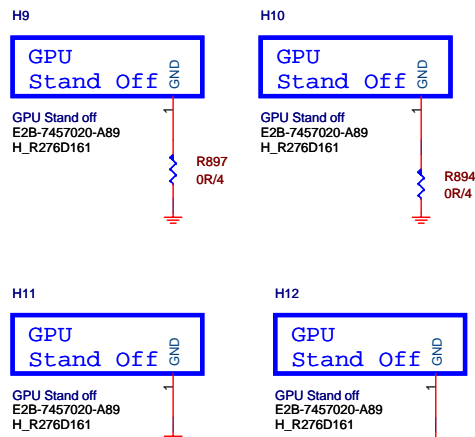


SB\_SINK  
footprint:HS\_37\_8X37\_8

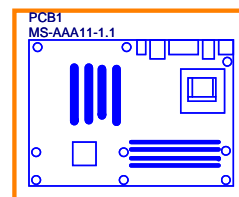
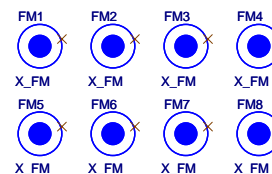
## CPU HOLE



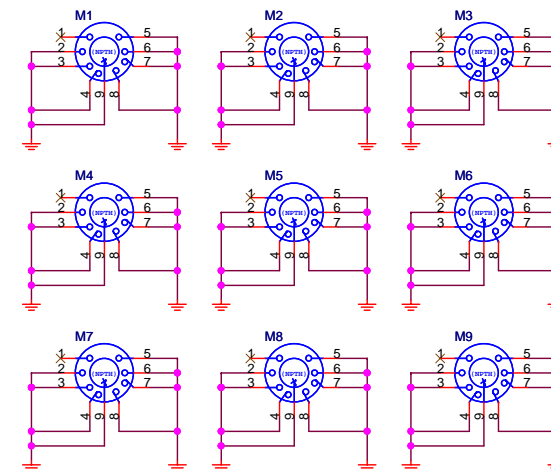
## GPU Stand off



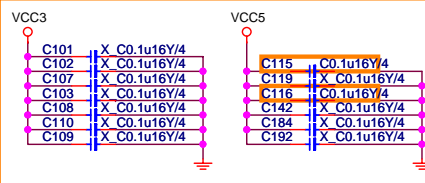
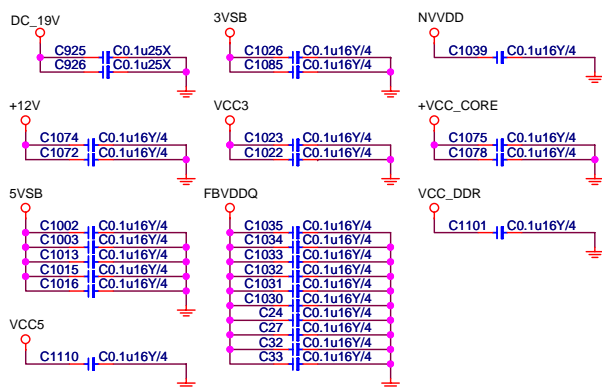
## Optical Fiducial Marks-120



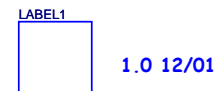
## Mounting Holes



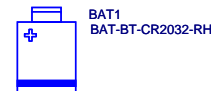
## EMI



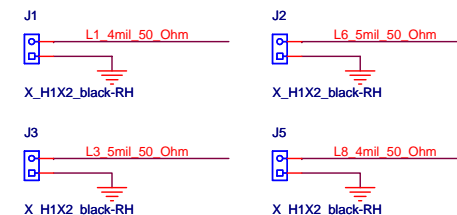
## BIOS label



## HDMI Royalty



## Single End 50ohm



MICRO-STAR INT'L CO.,LTD			
MS-AAA11			
Size B	Document Description	Rev 11	
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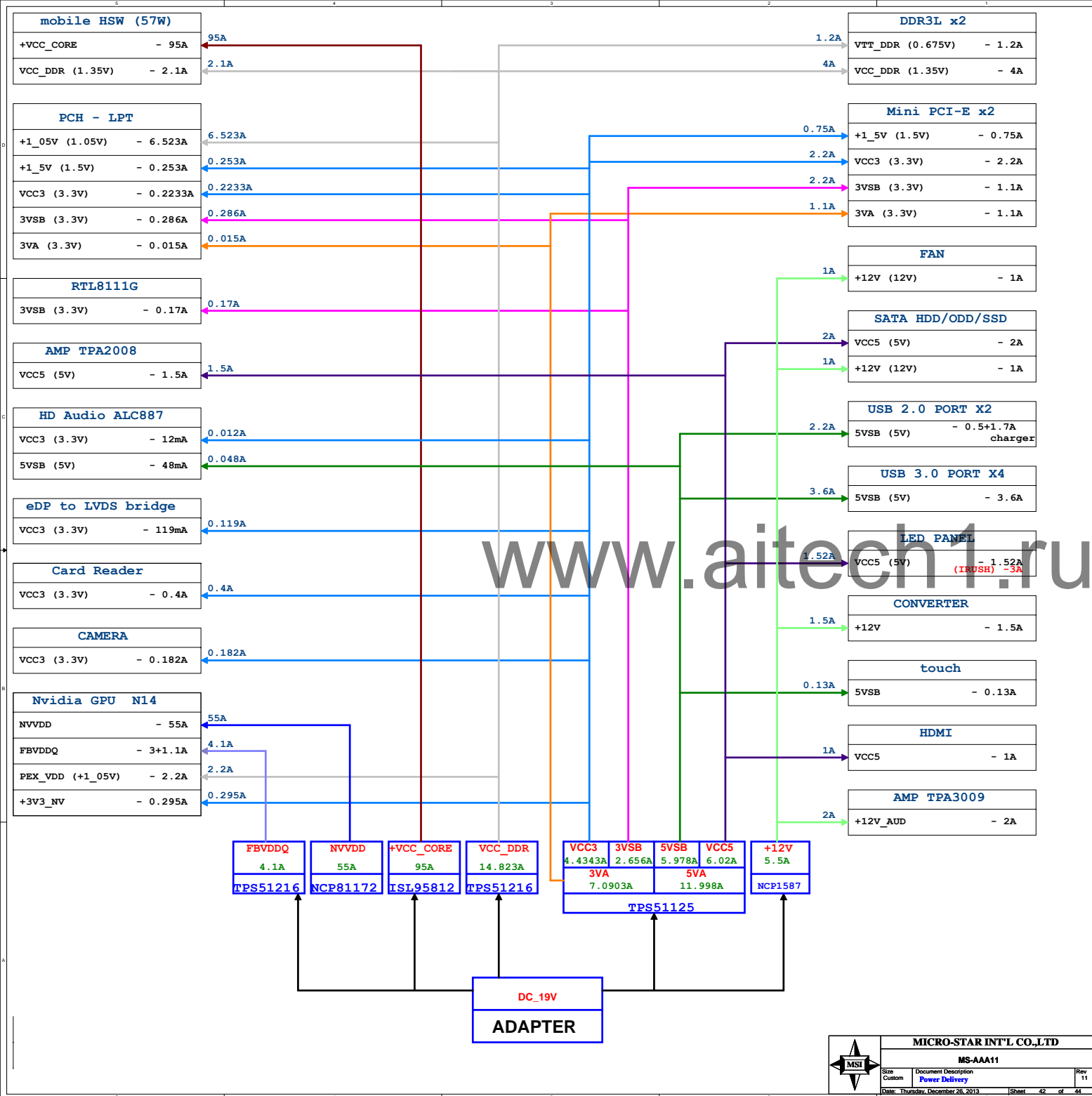


**Lynx Point (Mobile)**

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO0	BMBUSY#	I/O	CORE	Y	3.3V	GPI	PCH_GPIO0	Pull-up 10K to VCC3	No USE
GPIO1	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	PCH_GPIO1	Pull-up 10K to VCC3	No USE
GPIO2	PIRQE#	I/O	CORE	Y	5V	GPI	PCH_GPIO2	Pull-up 8.2K to VCC3	No USE
GPIO3	PIRQF#	I/O	CORE	Y	5V	GPI	PCH_GPIO3	Pull-up 8.2K to VCC3	No USE
GPIO4	PIRQG#	I/O	CORE	Y	5V	GPI	PCH_GPIO4	Pull-up 8.2K to VCC3	No USE
GPIO5	PIRQH#	I/O	CORE	Y	5V	GPI	PCH_GPIO5	Pull-up 8.2K to VCC3	No USE
GPIO6	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	EMITTER1	Pull-up 10K to VCC3	No USE
GPIO7	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	EMITTER2	Pull-up 10K to VCC3	No USE
GPIO8	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	PCH_GPIO8	N/A	No USE
GPIO9	OC5#	I/O	Suspend	Y	3.3V	Native	OC5#	Pull-up 10K to 3VSB	OC5#
GPIO10	OC6#	I/O	Suspend	Y	3.3V	Native	OC6#	Pull-up 10K to 3VSB	OC6#
GPIO11	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_SMBALERT#	Pull-up 10K to 3VSB	No USE
GPIO12	LAN_PHY_PWR_CTRL	I/O	DSW	Y	3.3V	Native	N/A	N/A	No USE
GPIO13	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	SIO_PME#	Pull-up 10K to 3VSB	PME#
GPIO14	OC7#	I/O	Suspend	Y	3.3V	Native	OC7#	Pull-up 10K to 3VSB	OC7#
GPIO15	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	TLSEN	N/A	No USE
GPIO16	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	Pull-UP 10K to VCC3	No USE
GPIO17	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	PCH_GPIO17	Pull-up 10K to VCC3	No USE
GPIO18	PCIECLKRQ1#	I/O	CORE	N	3.3V	Native	PCIE_CLKREQ#1	Pull-down 10K to GND	PCIECLKREQ1#
GPIO19	SATA1GP	I/O	CORE	Y	3.3V	GPI	PCH_GPIO19	Pull-up 10K to VCC3	No USE
GPIO20	PCIECLKRQ2# SMI#	I/O	CORE	N	3.3V	Native	PCIECLKREQ2#	Pull-down 10K to GND	PCIECLKREQ2#
GPIO21	SATA0GP	I/O	CORE	Y	3.3V	GPI	PCH_GPIO21	Pull-up 10K to VCC3	No USE
GPIO22	SCLOCK	I/O	CORE	Y	3.3V	GPI	PCH_GPIO22	Pull-up 10K to VCC3	No USE
GPIO23	LDRQ1#	I/O	CORE	N	3.3V	Native	LDRQ1#	N/A	No USE
GPIO24	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	N/A	No USE
GPIO25	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ3#	Pull-up 10K to 3VSB	No USE
GPIO26	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ4#	Pull-up 10K to 3VSB	No USE
GPIO27	Unmultiplexed	I/O	DSW	Y	3.3V	GPI	DSW_WAKE#	Pull-up 10K to 3VA	No USE
GPIO28	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PLL_ODVR_EN	N/A	No USE
GPIO29	SLP_LAN#	I/O	DSW	N	3.3V	Native	N/A	N/A	No USE
GPIO30	SUSWARN# SUSPWRDNACK	I/O	Suspend	N	3.3V	Native	SUSWARN#	Pull-up 10K to 3VSB	No USE
GPIO31	Unmultiplexed	I/O	DSW	N	3.3V	GPI	AC_PRESENT	Pull-up 10K to 3VA	No USE
GPIO32	only CLKRUN#	I/O	CORE	N	3.3V	GPO	PM_CLKRUN#	Pull-up 8.2K to VCC3	No USE
GPIO33	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	N/A	N/A	No USE
GPIO34	STP_PCI#	I/O	CORE	N	3.3V	GPI	PCH_GPIO34	Pull-up 10K to VCC3	No USE
GPIO35	NMI#	I/O	CORE	N	3.3V	GPO	CAMERA_EN	N/A	No USE
GPIO36	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	Pull-down 10K to GND	No USE
GPIO37	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	Pull-down 10K to GND	No USE
GPIO38	SLOAD	I/O	CORE	N	3.3V	GPI	PCH_GPIO38	Pull-up 10K to VCC3	No USE
GPIO39	SDATAOUT0	I/O	CORE	N	3.3V	GPI	PCH_GPIO39	Pull-up 10K to VCC3	No USE
GPIO40	OC1#	I/O	Suspend	N	3.3V	Native	USB_OC1#	Pull-up 10K to 3VSB	OC1#
GPIO41	OC2#	I/O	Suspend	N	3.3V	Native	USB_OC2#	Pull-up 10K to 3VSB	OC2#
GPIO42	OC3#	I/O	Suspend	N	3.3V	Native	USB_OC3#	Pull-up 10K to 3VSB	OC3#
GPIO43	OC4#	I/O	Suspend	Y	3.3V	Native	USB_OC4#	Pull-up about 3VSB	OC4#
GPIO44	PCIECLKRQ5#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ5#	Pull-up 10K to 3VSB	PCIECLKREQ5#
GPIO45	PCIECLKRQ6#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ6#	Pull-up 10K to 3VSB	PCIECLKREQ6#

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO46	PCIECLKRQ7#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ7#	Pull-up 10K to 3VSB	PCIECLKREQ7#
GPIO47	PEG_A_CLKRQ#	I/O	Suspend	N	3.3V	Native	PEG_CLKREQ#	Pull-down 10K to GND	PEG_A_CLKRQ#
GPIO48	SDATAOUT1	I/O	CORE	N	3.3V	GPI	PCH_GPIO48	Pull-up 10K to VCC3	No USE
GPIO49	SATA5GP TEMP_ALERT#	I/O	CORE	N	3.3V	GPI	PCH_GPIO49	Pull-up 10K to VCC3	No USE
GPIO50	Unmultiplexed	I/O	CORE	N	3.3V	GPI	DGPU_HOLD_RST#	Pull-up 10K to VCC3	No USE
GPIO51	Unmultiplexed	I/O	CORE	N	3.3V	GPO	BBS_BIT1	N/A	No USE
GPIO52	Unmultiplexed	I/O	CORE	N	3.3V	GPI	PCH_GPIO52	Pull-up 8.2K to VCC3	No USE
GPIO53	Unmultiplexed	I/O	CORE	N	3.3V	GPO	PCH_GPIO53	N/A	No USE
GPIO54	Unmultiplexed	I/O	CORE	N	3.3V	GPI	DGPU_PWR_EN#	Pull-up 10K to VCC3	No USE
GPIO55	Unmultiplexed	I/O	CORE	N	3.3V	GPO	PCH_GPIO55	N/A	No USE
GPIO56	PEG_B_CLKRQ#	I/O	Suspend	Y	3.3V	Native	PEGB_CLKRQ#	Pull-up 10K to 3VSB	PEG_B_CLKRQ#
GPIO57	Unmultiplexed	I/O	Suspend	Y	3.3V	GPI	PCH_GPIO57	Pull-up 10K to 3VSB	No USE
GPIO58	SML1CLK	I/O	Suspend	N	3.3V	Native	PCH_SML1_CLK	Pull-up 2.2K to 3VSB	SML1CLK
GPIO59	OC0#	I/O	Suspend	N	3.3V	Native	USB_OC0#	Pull-up 10K to 3VSB	OC0#
GPIO60	SML0ALERT#	I/O	Suspend	Y	3.3V	Native	DRAMRST_CNTRL_PCH	Pull-up 10K to 3VSB	No USE
GPIO61	SUS_SATA#	I/O	Suspend	N	3.3V	Native	SUS_STAT#	N/A	No USE
GPIO62	SUSCLK	I/O	Suspend	N	3.3V	Native	SUS_CLK	N/A	No USE
GPIO63	SLP_S5#	I/O	Suspend	N	3.3V	Native	SLP_S5#	N/A	No USE
GPIO64	CLKOUTFLEX0	I/O	CORE	N	3.3V	Native	TP_CLKOUTFLEX0	N/A	No USE
GPIO65	CLKOUTFLEX1	I/O	CORE	N	3.3V	Native	CLKOUTFLEX1	N/A	CLK48M
GPIO66	CLKOUTFLEX2	I/O	CORE	N	3.3V	Native	TP_CLKOUTFLEX2	N/A	No USE
GPIO67	CLKOUTFLEX3	I/O	CORE	N	3.3V	Native	TP_CK_48M_FLEX3	N/A	No USE
GPIO68	Unmultiplexed	I/O	CORE	N	3.3V	GPI	DGPU_PWR_EN	Pull-up 10K to VCC3	DGPU_PWR_EN
GPIO69	Unmultiplexed	I/O	CORE	N	3.3V	GPI	PCH_GPIO69	Pull-up 10K to VCC3	No USE
GPIO70	Unmultiplexed	I/O	CORE	N	3.3V	Native	PCH_GPIO70	Pull-up 10K to VCC3	No USE
GPIO71	Unmultiplexed	I/O	CORE	N	3.3V	Native	PCH_GPIO71	Pull-up 10K to VCC3	No USE
GPIO72	BATLOW#	I/O	DSW	N	3.3V	Native	PM_BATLOW#	Pull-up 10K to 3VSB	No USE
GPIO73	PCIECLKRQ0#	I/O	Suspend	N	3.3V	Native	PCIE_CLKREQ#0	Pull-down 10K to GND	PCIECLKREQ0#
GPIO74	SML1ALERT# PCHHOT#	I/O	Suspend	N	3.3V	Native	PCH_SML1ALERT#	Pull-up 10K to 3VSB	No USE
GPIO75	SML1DATA	I/O	Suspend	N	3.3V	Native	PCH_SML1_DATA	Pull-up 10K to 3VSB	SML1DATA





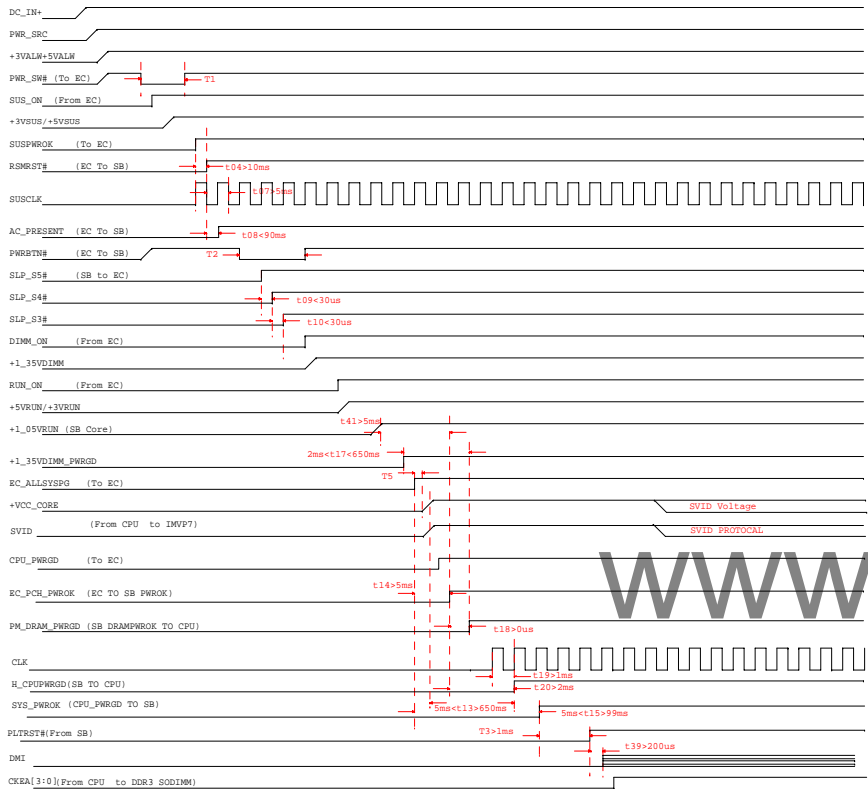
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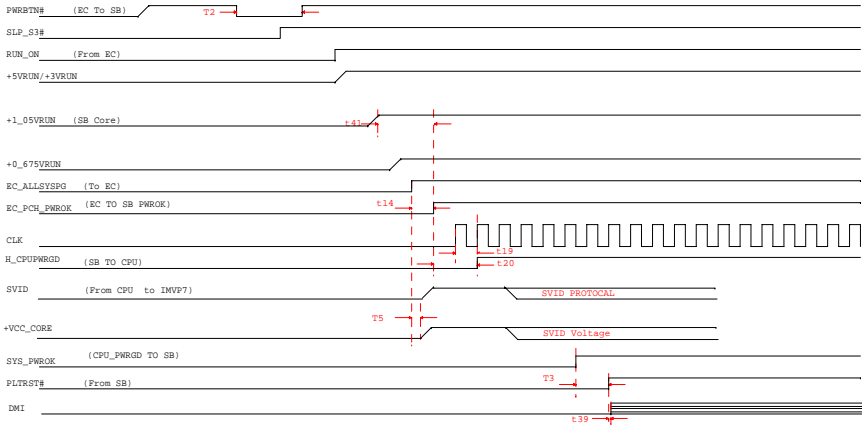
Size Custom Document Description Power Delivery Rev 11  
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Power on Sequence

S5-S0  
EC programming timing



S3-S0  
EC programming timing



	Min	Max	Unit	Description
T1	150		mS	
T2	16		mS	
T3	1		mS	Timing set by PCH
t04	10		mS	
t07	100		mS	
t08		90	mS	
t09	30		uS	
t10	30		uS	
t13	5	650	mS	
t14	5		mS	
t17	2	650	mS	
t18	1		mS	Timing set by PCH
t19	41		mS	Timing set by PCH
t20	2		mS	Timing set by PCH
T5		5	mS	Follow MVP Spec
t39		200	uS	
t41	10		mS	

AAA11-10\_0617.DSN copy from AAA11-0A\_0422\_1.DSN  
1.83\_GAT28 change to Q225,unstuff R476 p.16,27  
2.stuff R252,unstuff R447,R284,R189,Q102,Q103,Q104 for RKL off p.18  
3.unstuff R491,change R51 to 10K,change Q80 connection,add Q105 to PD#  
  reserve MCH\_ON# to PD# for panel off p.13,18,21  
4.reserve R528,R529,R530 for power meter p.24  
5.add VPM\_PGD to VCC3 p.28  
6.change R424 to 2.55K for fine tune 3W4ohm p.19  
7.change ESD to HDMI\_VCC5 p.17  
8.unstuff C908,R545,R559,R230,R544,U29,change R175 to 4.99K for VBIOS to SBIOS p.32  
9.unstuff R780,R781,R335,R419 for redundant p.16  
10.reserve SDIM# for audio issue p.9  
11.modify R457,R451,R454,R450,R520,C151for power team p.28  
12.change FCH1 to MP p/n p.9-15  
13.unstuff R765 for GP04 FP type p.16  
14.change HDMI Royalty p.40  
15.change Q36,Q43,Q75,Q84,Q81,Q147 to D03-7002R89-R06 p.6,17,23  
16.change U100 to VCC3 p.24  
17.reserve MSCL/MSDA to VCC3 p.16  
18.reserve SIOATCH SMBus to eDP p.16,18  
19.2008 colay 3009 for 24V5W p.19  
20.change webcam & touch IIS connector for stupid p.21  
21.change JDMIC1,JMIC1,JAMP1 for stupid p.19  
22.unstuff SYNC component p.18  
23.change GPU stand off footprint p.40  
24.add +12V current to 5.5A for 3009 p.24  
25.del C836 change C219 to 1u p.24  
26.move bkl control to enable control p.18  
27.add U1,U2,U3,U4 for EMI p.9,21  
28.recover GPU stand off footprint p.40  
AAA11-10\_0626.DSN  
29.swap U3404 for layout p.9  
AAA11-10\_0626\_1.DSN  
30.swap U1602 for layout p.21  
AAA11-10\_0626\_2.DSN  
31.reserve VCC3,VCC5 to GND C p.40  
AAA11-10\_0628.DSN  
32.del C199 for RF p.40  
33.modify SML0 for NFC p.10  
AAA11-10\_0702.DSN  
34.del power meter circuit p.16,24  
35.change PCB1 to 1.0 p.40  
36.ASM upload OK  
37.unstuff NFC p.21  
38.unstuff COM p.16  
AAA11-10\_0702\_N14M.DSN  
39.stuff R178,R187,R194,R211  
  unstuff R175,R177,R192,R193,R381  
  change R180,R190,R197,R208 to 10K  
  for n14m-ge p.32  
40.change R579 to 120ohm bead for n14m-ge p.30  
41.change G1 to n14m-ge p.30-34  
42.change U8 to normal pn p.18  
AAA11-10\_0702\_N14M\_1.DSN  
43.change VRAM to hynix p.35,36  
44.unstuff R190,R194,R197,R211 unstuff R192,R193,R195,R196 p.32  
AAA11-10\_0702\_N14M\_2.DSN  
45.panel on/off by SMBus,unstuff U15,U24 p.28  
46.fine tune GPU PWM enable R855 to 47K,R857 to 0.1u p.39  
AAA11-10\_0702\_N14M\_3.DSN  
47.change VRAM to 1G p.35,36  
48.strapping 1100(0xC) for hynix 1G VRAM p.32  
49.stuff mSATA circuit p.23  
AAA11-10\_0702\_N14M\_4.DSN  
50.change HMB6 to C2 stepping p.9-15  
AAA11-10\_0702\_N14M\_5.DSN  
51.unstuff VGA p.11,17  
52.change DIMM to GND p.7  
AAA11-10\_0702\_N14M\_6.DSN  
53.stuff C492,C437,C278,C280, change R638 for EMI p.19  
54.stuff C115,C116 for EMI p.40  
AAA11-10\_0702\_N14M\_7.DSN  
55.change G1 to Haier consign p.  
AAA11-10\_0702\_N14M\_8.DSN  
56.change Touch power to normal p.21

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